

COMPAL CONFIDENTIAL

MODEL NAME : CDP81  
PCB NO : LA-E153P  
BOM P/N :  
GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 15 DSC (non-TBT)

Kabylake H


2016-07-01

REV : 0.2 (X01)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESD Component
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- XDP@ : XDP Component
- CONN@ : Connector Component

| MB PCB      |                                |
|-------------|--------------------------------|
| Part Number | Description                    |
| DAA000CN000 | PCB 1SE LA-E153P REV0 MB DSC 1 |

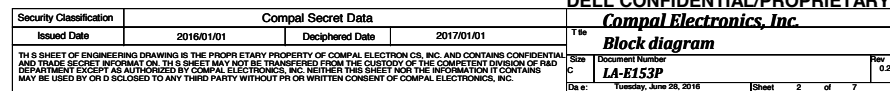
Layout Dell logo



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|   |  |                    |  | LA-E153P                      |  |
|   |  |                    |  | Date                          |  |
|   |  |                    |  | Friday, July 01, 2016         |  |
|   |  |                    |  | Sheet 1 of 74                 |  |
|   |  |                    |  | Rev 0.2                       |  |

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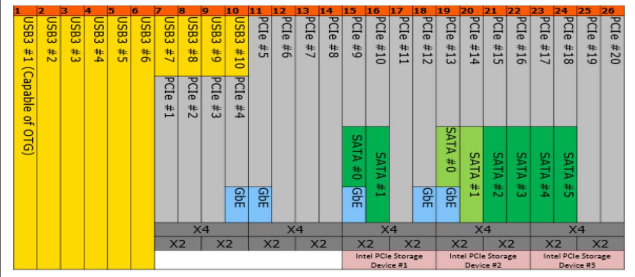
POWER STATES

| Signal<br>State              | SLP<br>S3# | SLP<br>S4# | SLP<br>S5# | SLP<br>A# | ALWAYS<br>PLANE | M<br>PLANE | SUS<br>PLANE | RUN<br>PLANE | CLOCKS |
|------------------------------|------------|------------|------------|-----------|-----------------|------------|--------------|--------------|--------|
| S0 (Full ON) / M0            | HIGH       | HIGH       | HIGH       | HIGH      | ON              | ON         | ON           | ON           | ON     |
| S3 (Suspend to RAM) / M3     | LOW        | HIGH       | HIGH       | HIGH      | ON              | ON         | ON           | OFF          | OFF    |
| S4 (Suspend to DISK) / M3    | LOW        | LOW        | HIGH       | HIGH      | ON              | ON         | OFF          | OFF          | OFF    |
| S5 (SOFT OFF) / M3           | LOW        | LOW        | LOW        | HIGH      | ON              | ON         | OFF          | OFF          | OFF    |
| S3 (Suspend to RAM) / M-OFF  | LOW        | HIGH       | HIGH       | LOW       | ON              | OFF        | ON           | OFF          | OFF    |
| S4 (Suspend to DISK) / M-OFF | LOW        | LOW        | HIGH       | LOW       | ON              | OFF        | OFF          | OFF          | OFF    |
| S5 (SOFT OFF) / M-OFF        | LOW        | LOW        | LOW        | LOW       | ON              | OFF        | OFF          | OFF          | OFF    |

PM TABLE

| power plane<br>State   | +5V_ALW<br>+3.3V_ALW<br>+3.3V_ALW_DSW<br>+3.3V_ALW_PCH<br>+RTC_CELL<br>+1.8V_PRIM<br>+1.0V_PRIM<br>+1.0V_PRIM_CORE<br>+5V_ALW2<br>+3.3V_ALW2<br>+3.3V_RTC_LDO<br>+1.0V_MPHYGT | +3.3V_SUS<br>+1.2V_MEM<br>+1.0V_VCCST<br>+2.5V_MEM | +5V_RUN<br>+3.3V_RUN<br>+0.6V_DDR_VTT<br>+1.2V_RUN<br>+VCC_CORE<br>+VCC_GT<br>+1.0VS_VCCIO<br>+VCC_SA<br>+1.8V_RUN |
|------------------------|---|--|--|
| S0                     | ON  | ON   | ON   |
| S3                     | ON  | ON   | OFF  |
| S5 S4/AC               | ON  | OFF  | OFF  |
| S5 S4/AC doesn't exist | OFF   | OFF  | OFF  |

| Layer No.                       | Name    | Er  | Material    | Thickness (Material SPEC.) Unit : mil | Thickness (Actuality) Unit : mil |
|---------------------------------|---------|-----|-------------|---------------------------------------|----------------------------------|
|                                 |         |     | SolderMask  | IT-158                                | 0.5                              |
|                                 |         |     | Add Plating |                                       |                                  |
| 1                               | Top     |     | Copper foil | 0.5oz+plating                         | 1.5                              |
|                                 |         | 3.8 | Prepreg     | 1080                                  | 2.6                              |
| 2                               | GND     |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.7 | Core        | 4mil                                  | 3.87                             |
| 3                               | IN 1    |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.7 | Prepreg     | 2116H                                 | 4.3                              |
| 4                               | GND/PWR |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.7 | Core        | 4mil                                  | 3.87                             |
| 5                               | IN 2    |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.6 | Prepreg     | 1080H x2 or PP2116HRC                 | 4.2                              |
| 6                               | IN 3    |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.7 | Core        | 4mil                                  | 3.87                             |
| 7                               | GND/PWR |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.8 | Prepreg     | 2116H                                 | 4.3                              |
| 8                               | IN 4    |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.7 | Core        | 4mil                                  | 3.87                             |
| 9                               | GND     |     | Copper foil | 1oz                                   | 1.25                             |
|                                 |         | 3.8 | Prepreg     | 1080                                  | 2.6                              |
| 10                              | Bottom  |     | Copper foil | 0.5oz+plating                         | 1.5                              |
|                                 |         |     | Add Plating |                                       |                                  |
|                                 |         |     | SolderMask  | IT-158                                | 0.5                              |
| Overall Thickness (1.2mm ± 10%) |         |     |             |                                       | 47.68000<br>1.211072             |



| USB3.0    | SSIC   | PCIE    | SATA    | DESTINATION  |
|-----------|--------|---------|---------|--|
| USB3.0-1  |        |         |         | JUSB3-->Rear   |
| USB3.0-2  | SSIC-1 |         |         | JNGFF2-->M2 3042(LTE)                                    |
| USB3.0-3  | SSIC-2 |         |         | JUSB1-->Right  |
| USB3.0-4  |        |         |         | JUSB2-->Left   |
| USB3.0-5  |        |         |         | NA   |
| USB3.0-6  |        |         |         | NA   |
| USB3.0-7  |        | PCIE-1  |         | JNGFF1-->M.2 3030(WIGIG)                                 |
| USB3.0-8  |        | PCIE-2  |         | JNGFF1-->M.2 3030(WLAN)                                  |
| USB3.0-9  |        | PCIE-3  |         | Card Reader  |
| USB3.0-10 |        | PCIE-4  |         | LOM  |
|           |        | PCIE-5  |         | NA   |
|           |        | PCIE-6  |         |  |
|           |        | PCIE-7  |         |  |
|           |        | PCIE-8  |         |  |
|           |        | PCIE-9  | SATA-0A | M.2 Socket 3 (Key M)<br>M.2 2280 SSD<br>(PCIex4 or SATA) |
|           |        | PCIE-10 | SATA-1A |  |
|           |        | PCIE-11 |         |  |
|           |        | PCIE-12 |         |  |
|           |        | PCIE-13 | SATA-0B | NA   |
|           |        | PCIE-14 | SATA-1B | NA   |
|           |        | PCIE-15 | SATA-2  | JSATA1-->HDD SATA  |
|           |        | PCIE-16 | SATA-3  | NA   |
|           |        | PCIE-17 | SATA-4  | M.2 3042 (HCA or QCA LTE) SSD Cache                      |
|           |        | PCIE-18 | SATA-5  | M.2 3042 (HCA or QCA LTE) SSD Cache                      |
|           |        | PCIE-19 |         | NA   |
|           |        | PCIE-20 |         | NA   |

| USB PORT# | DESTINATION            |
|-----------|------------------------|
| 1         | JUSB3-->Rear           |
| 2         | JUSB1-->Right          |
| 3         | JUSB2-->Left           |
| 4         | Type C                 |
| 5         | NA                     |
| 6         | JNGFF1--> M.2 3030(BT) |
| 7         | NA                     |
| 8         | JNGFF2-->M2 3042(WWAN) |
| 9         | JEDP1-->Touch Screen   |
| 10        | JUSH1-->USH            |
| 11        | JEDP1-->Camera         |
| 12        | NA                     |

|     |   |     |
|-----|---|-----|
| USH | H | BIO |
|-----|---|-----|

| VIDEO |         | DESTINATION      |
|-------|---------|------------------|
| eDP   |         | LCD              |
| DDI-B |         | JHDMI1           |
| DDI-C |         | Type-C           |
| DDI-D | DeMux 1 | M.2 3030 (WiGig) |
|       |         | MB VGA           |

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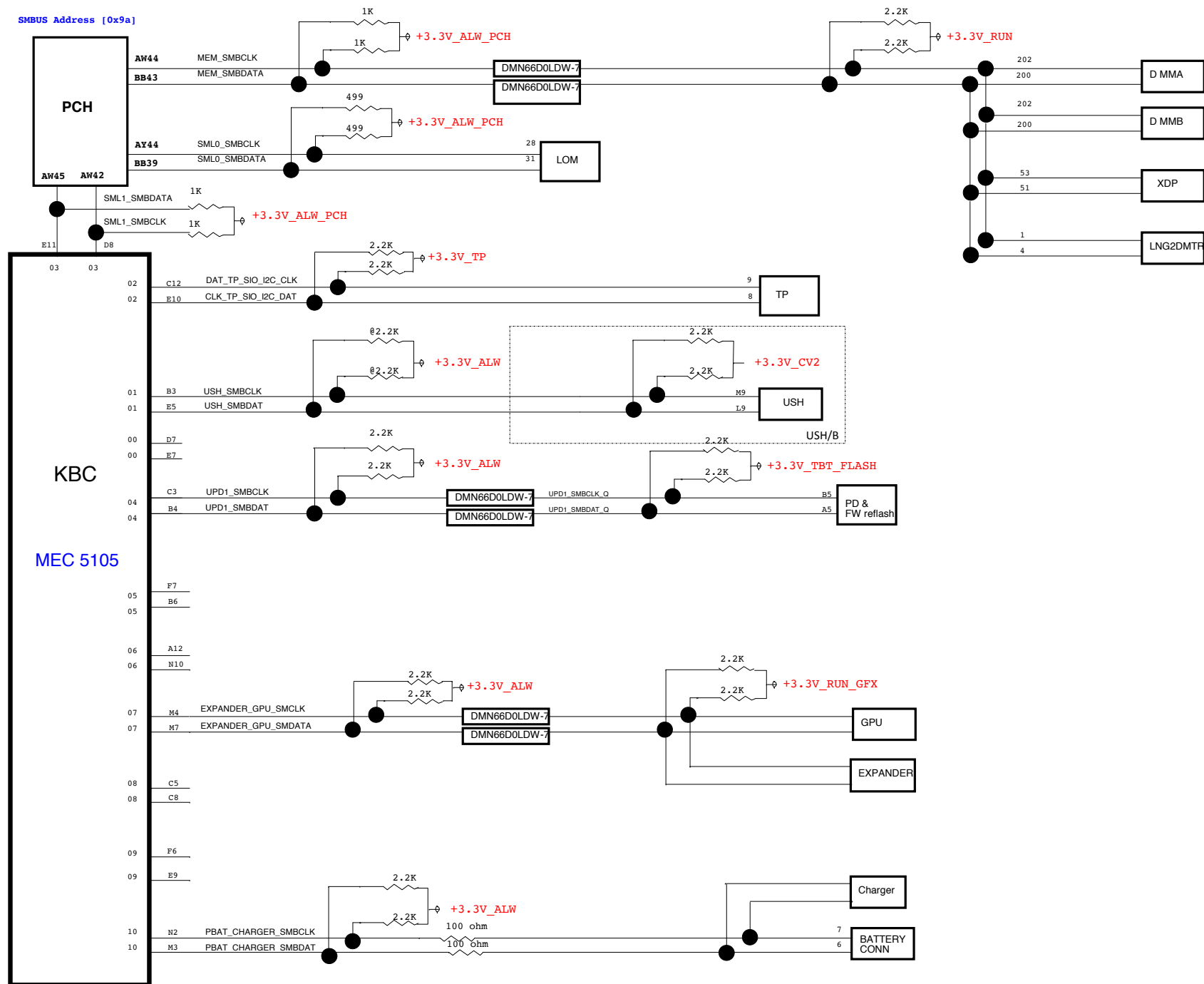
Port Assignment

|        |                        |  |               |
|--------|------------------------|--|---------------|
| Title  | Document Number        |  | Rev           |
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| Date   | Tuesday, June 28, 2016 |  | Sheet 3 of 74 |

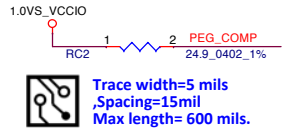
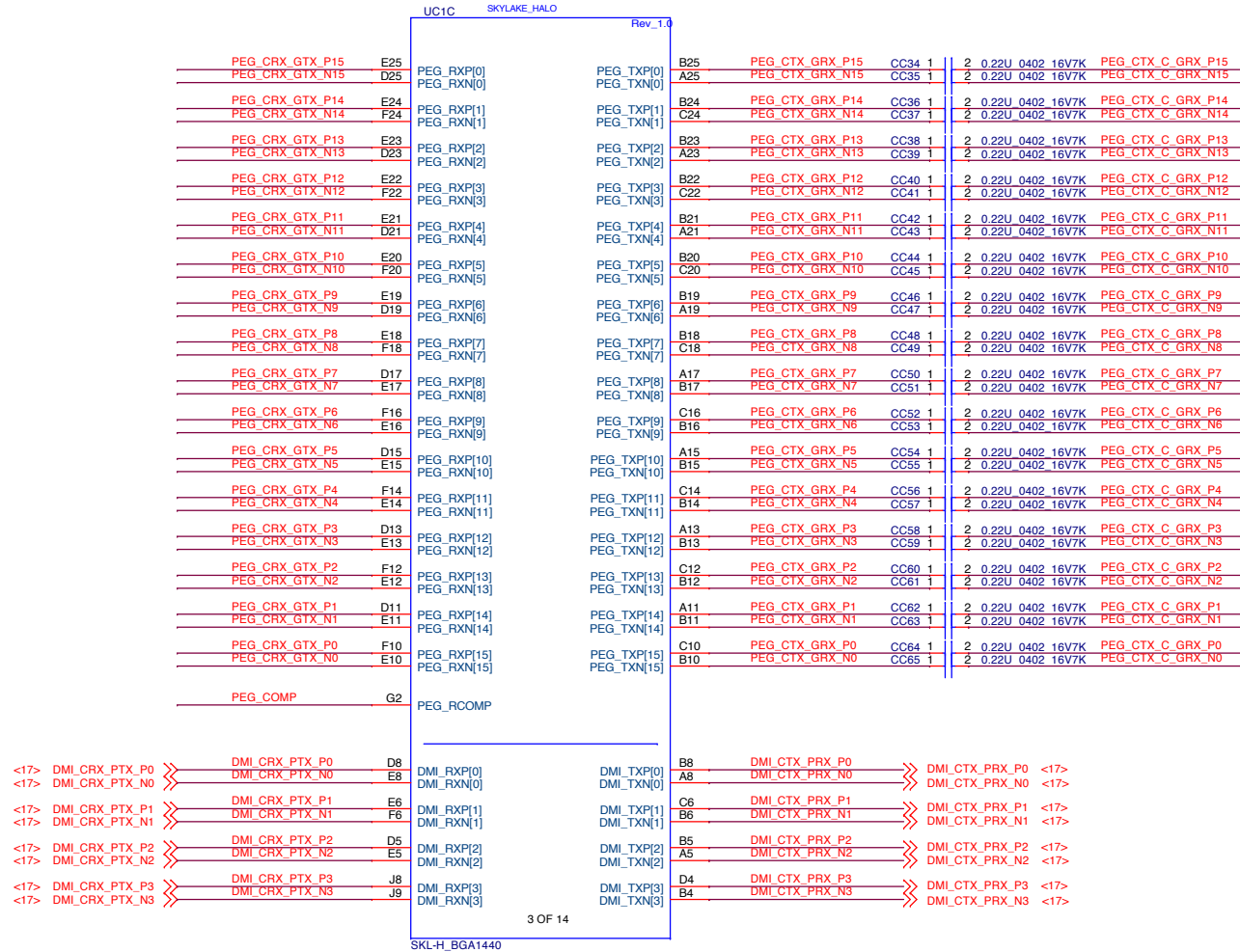
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SMBUS Address [0x9a]



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PEG\_CRX\_GTX\_N[0..15] << PEG\_CRX\_GTX\_N[0..15] <47>  
PEG\_CTX\_C\_GRX\_P[0..15] >> PEG\_CTX\_C\_GRX\_P[0..15] <47>  
PEG\_CTX\_C\_GRX\_N[0..15] >> PEG\_CTX\_C\_GRX\_N[0..15] <47>



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Title  
KBL-H (1/8)

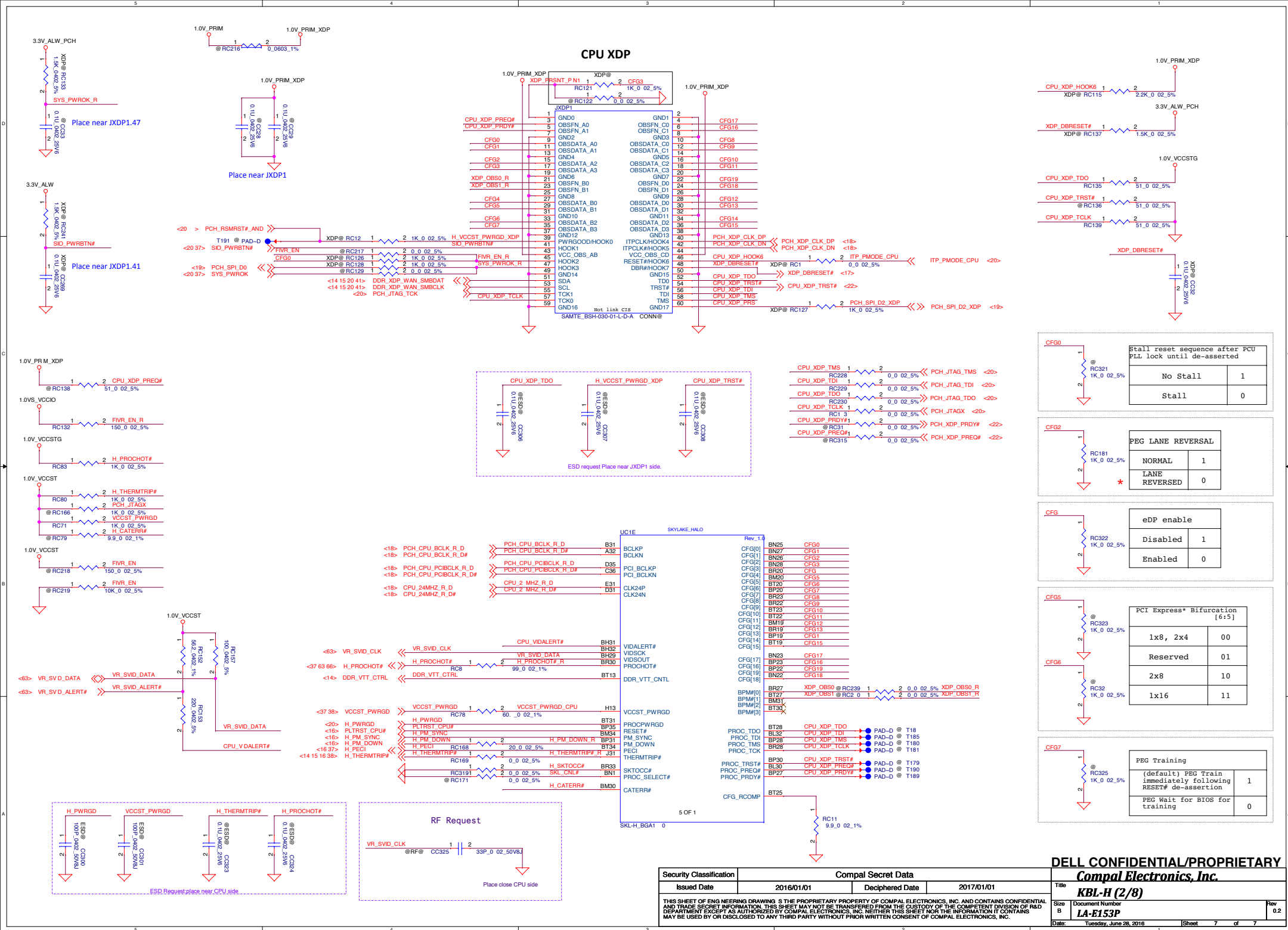
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0.2

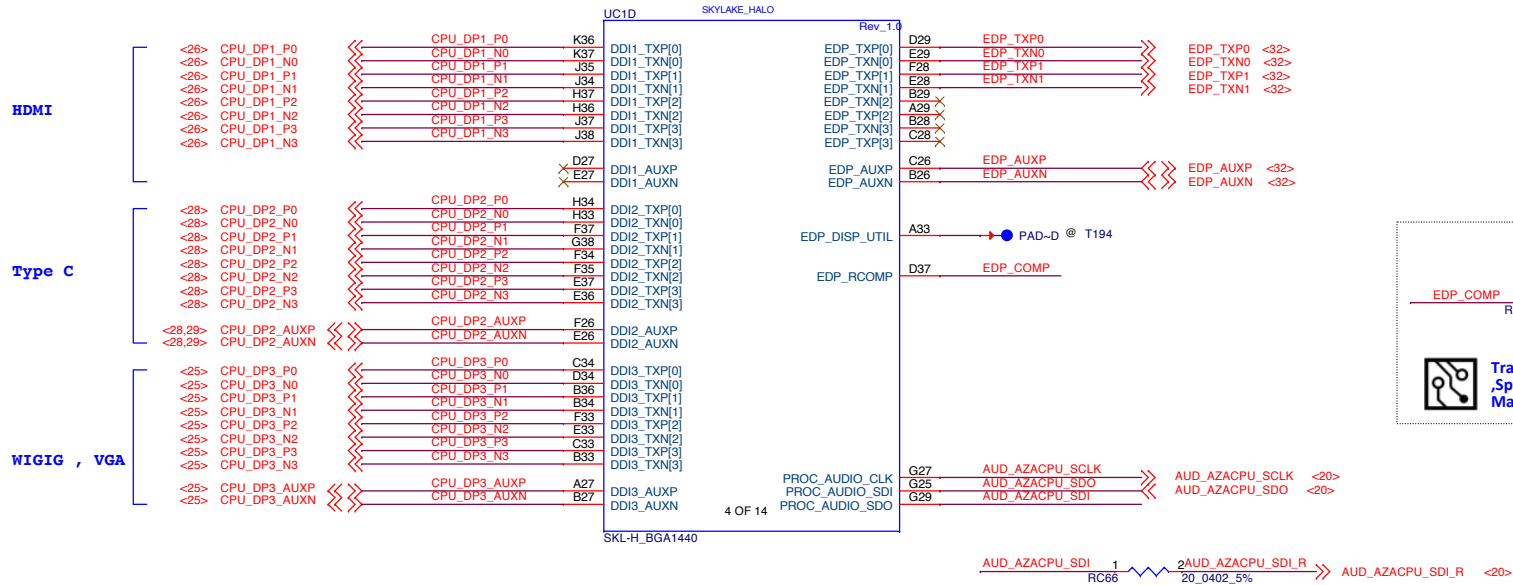
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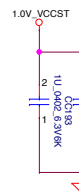




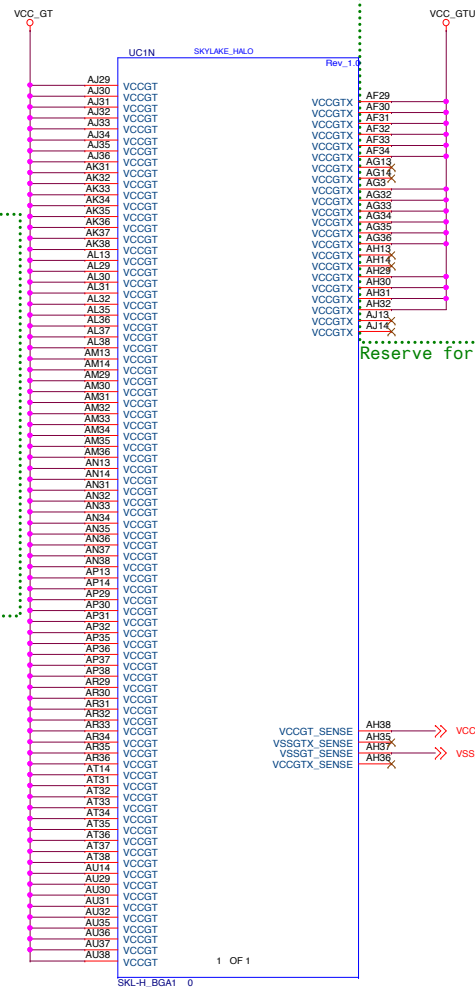
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|                         |  |  |  |                    |  |                 |  |                               |  | KBL-H (4/8)            |  |
|                         |  |  |  |                    |  |                 |  |                               |  | LA-E153P               |  |
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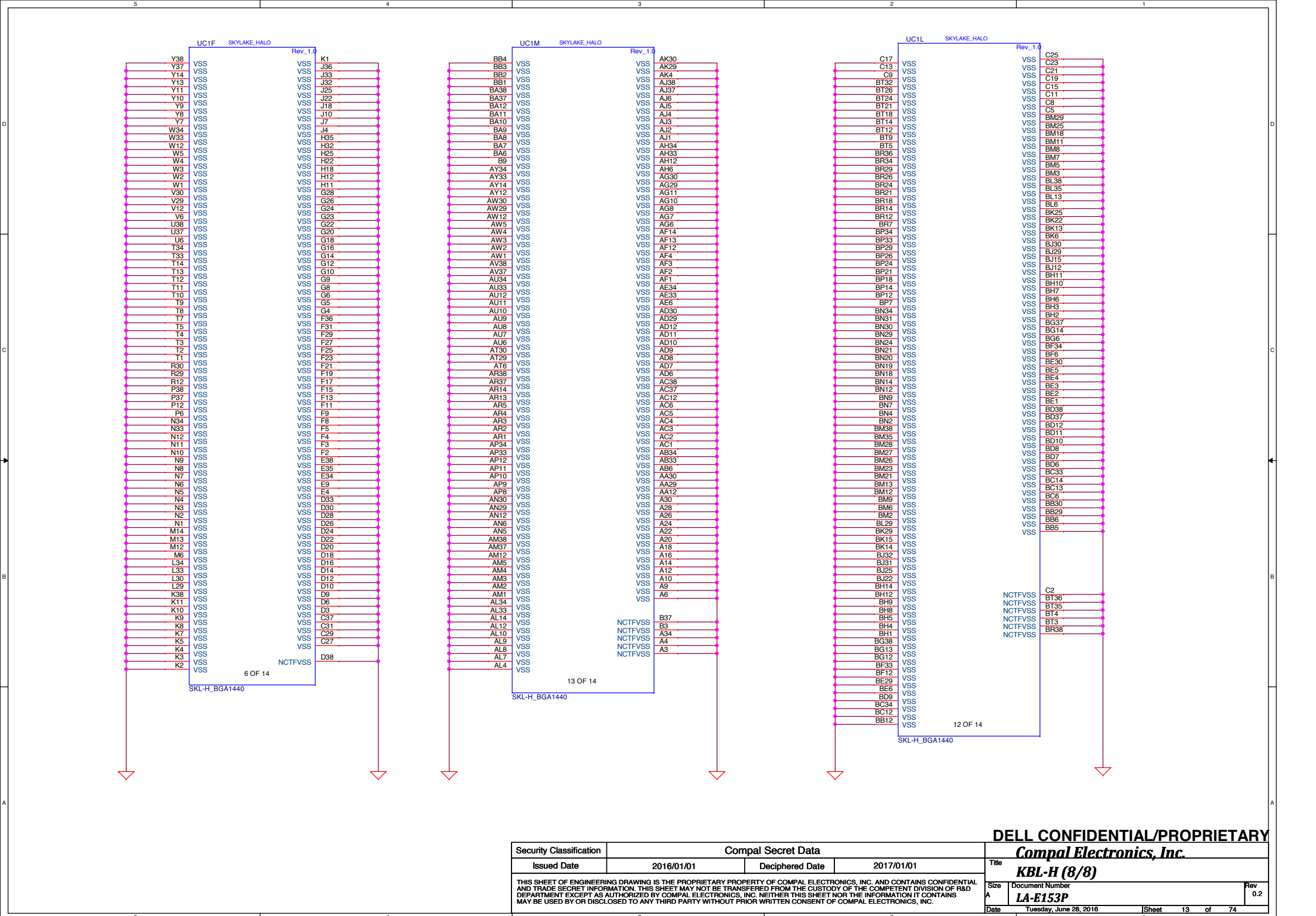






Remove to Power (+VCC\_SA cap)





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Title  
KBL-H (8/8)

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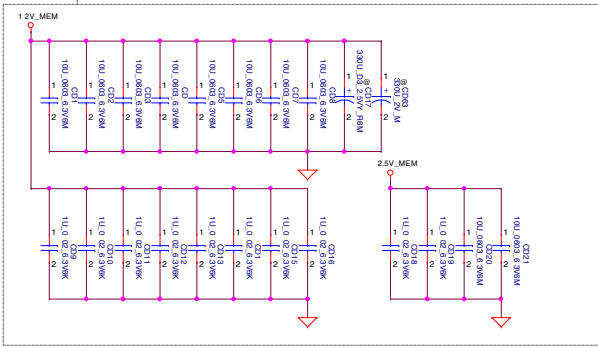
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Issued Date 2016/01/01 Deciphered Date 2017/01/01

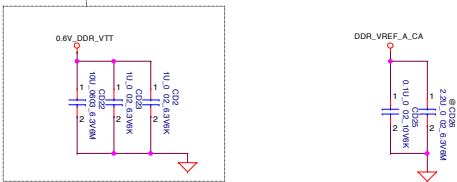
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<=> DDR\_A\_CB0..7  
 <=> DDR\_A\_DQS#0..8  
 <=> DDR\_A\_DQ0..15  
 <=> DDR\_A\_DQ16..31  
 <=> DDR\_A\_DQ32..47  
 <=> DDR\_A\_DQ48..63  
 <=> DDR\_A\_MA0..16

Layout Note:  
Place near J1MM1



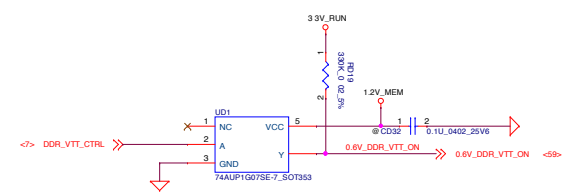
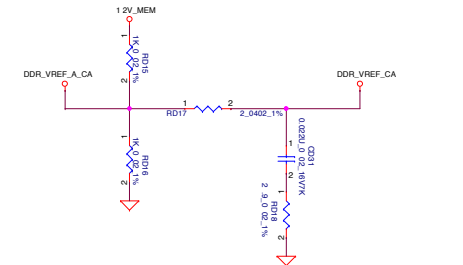
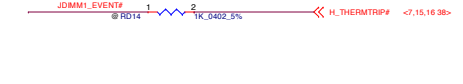
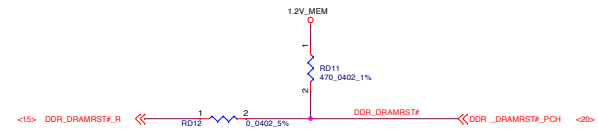
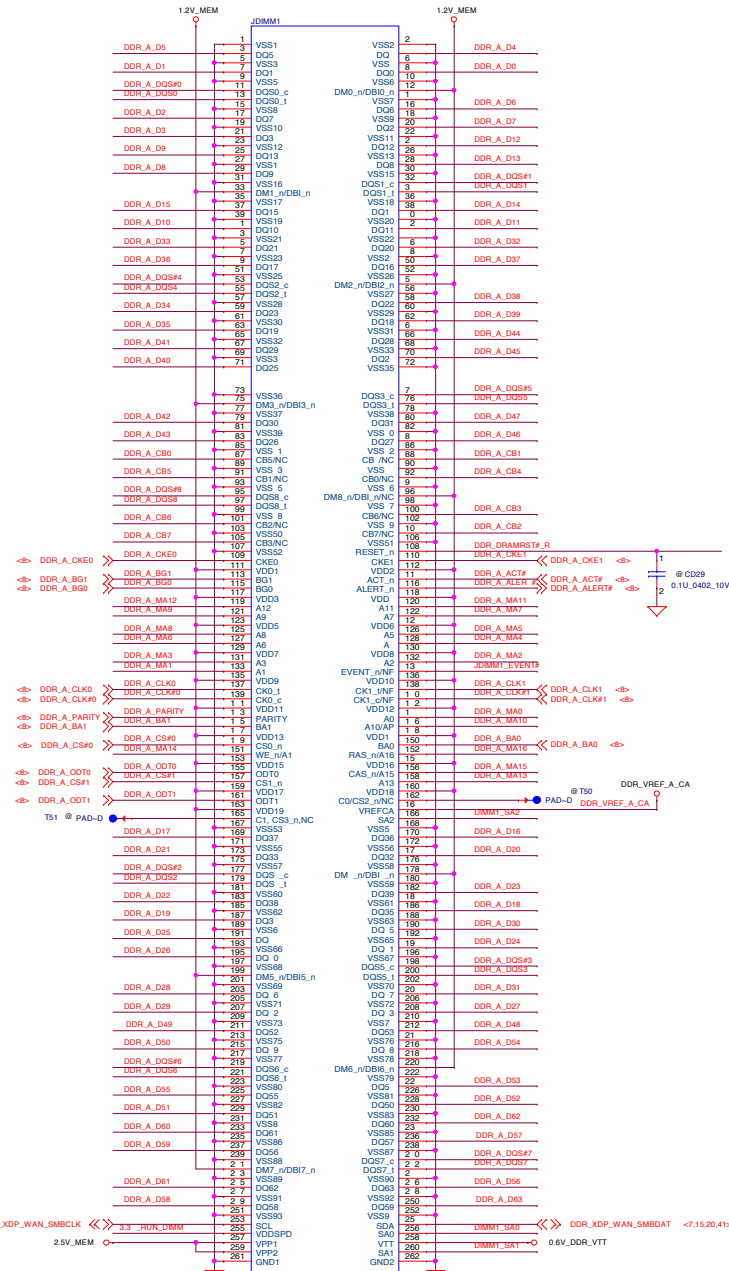
Layout Note:  
Place near J1MM1.258



### DIMM Select

|         | SA0 | SA1 | SA2 |
|---------|-----|-----|-----|
| * DIMM1 | 0   | 0   | 0   |
| DIMM2   | 1   | 0   | 0   |
| DIMM3   | 0   | 1   | 0   |
| DIMM4   | 1   | 1   | 0   |

|           |           |             |
|-----------|-----------|-------------|
| Byte[0]   | DQ[7:0]   | DQS/DQS#[0] |
| Byte[1]   | DQ[15:8]  | DQS/DQS#[1] |
| Byte[2]   | DQ[23:16] | DQS/DQS#[2] |
| * Byte[3] | DQ[31:24] | DQS/DQS#[3] |
| Byte[4]   | DQ[39:32] | DQS/DQS#[4] |
| * Byte[5] | DQ[47:40] | DQS/DQS#[5] |
| Byte[6]   | DQ[55:48] | DQS/DQS#[6] |
| Byte[7]   | DQ[63:56] | DQS/DQS#[7] |

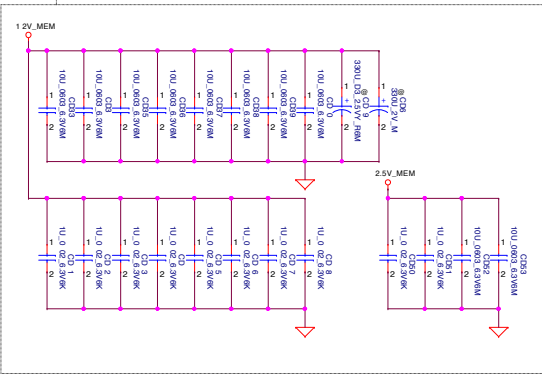


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 DDR4-SODIMM SLOT1

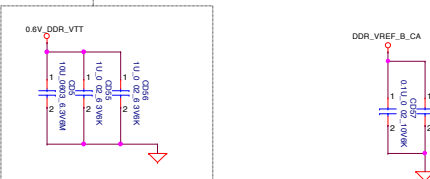
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<-> DDR\_B\_CB0[7]  
 <-> DDR\_B\_DQS#0[8]  
 <-> DDR\_B\_DQ[15]  
 <-> DDR\_B\_D16[31]  
 <-> DDR\_B\_D32[47]  
 <-> DDR\_B\_D48[63]  
 <-> DDR\_B\_MA0[16]

Layout Note:  
Place near JDIMM2

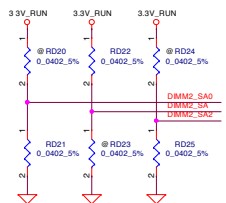


Layout Note:  
Place near JDIMM2.258

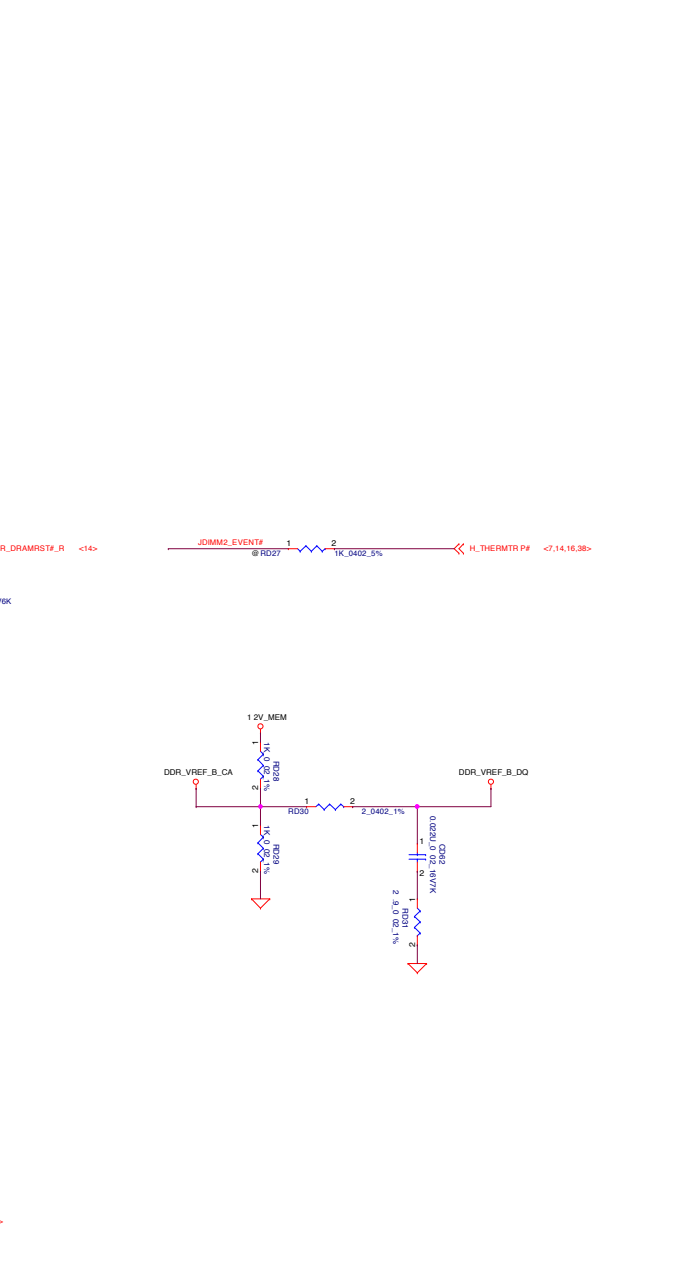
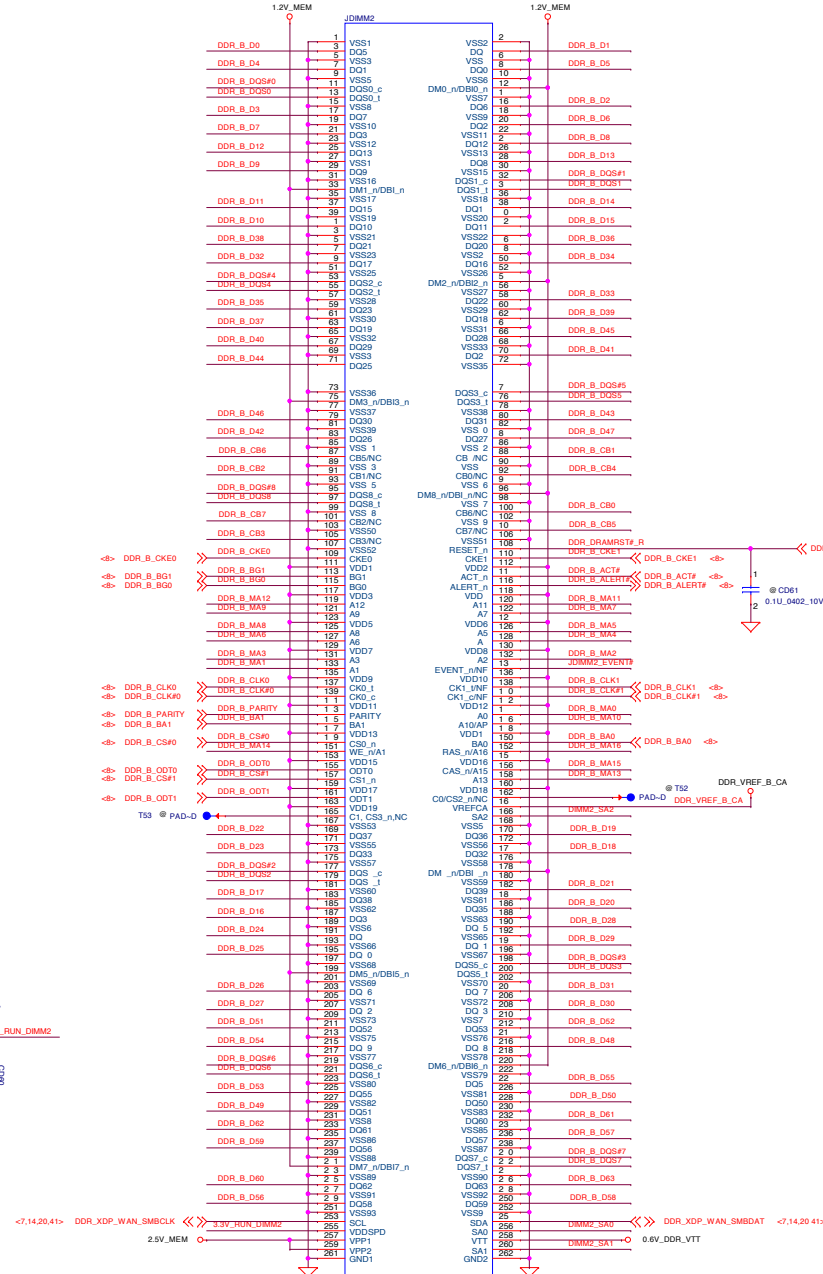


### DIMM Select

|       | SA0 | SA1 | SA2 |
|-------|-----|-----|-----|
| DIMM1 | 0   | 0   | 0   |
| DIMM2 | 1   | 0   | 0   |
| DIMM3 | 0   | 1   | 0   |
| DIMM4 | 1   | 1   | 0   |



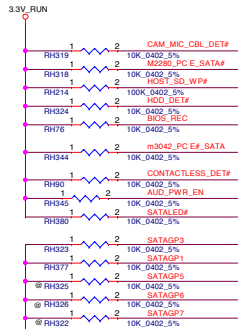
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|---------|-----------|-------------|
| Byte[0] | DQ[7:0]   | DQS/DQS#[0] |
| Byte[1] | DQ[15:8]  | DQS/DQS#[1] |
| Byte[2] | DQ[23:16] | DQS/DQS#[2] |
| Byte[3] | DQ[31:24] | DQS/DQS#[3] |
| Byte[4] | DQ[39:32] | DQS/DQS#[4] |
| Byte[5] | DQ[47:40] | DQS/DQS#[5] |
| Byte[6] | DQ[55:48] | DQS/DQS#[6] |
| Byte[7] | DQ[63:56] | DQS/DQS#[7] |



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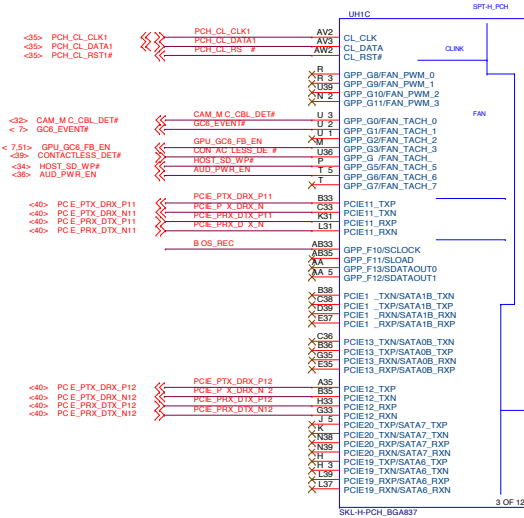
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M.2 Socket 3 (Key M)

M.2 Socket 3 (Key M)



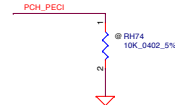
M.2 Socket 3 (Key M)

SATA HDD

M.2 3042 HCA or QCA LTE SSD Cache

M.2 3042 HCA or QCA LTE SSD Cache

|        |   |                 |        |        |
|--------|---|-----------------|--------|--------|
| SP5GP0 | 1 | 2280_PCIE_SATA# | 0=SATA | 1=PCIE |
| SP5GP1 | 0 | SATAGP1         | 1=SATA | 0=PCIE |
| SP5GP2 | 1 | HDD_DET#        | 0=SATA | 1=PCIE |
| SP5GP3 | 0 | SATAGP3         | 1=SATA | 0=PCIE |
| SP5GP4 | 1 | 3042_PCIE#_SATA | 1=SATA | 0=PCIE |

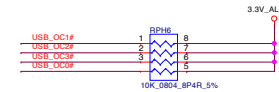
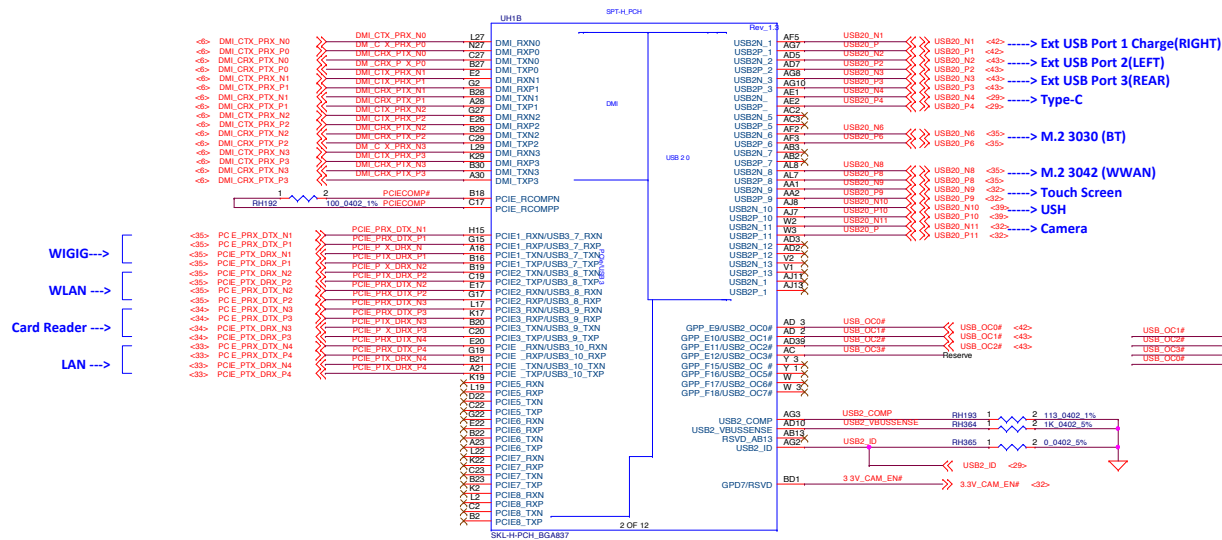
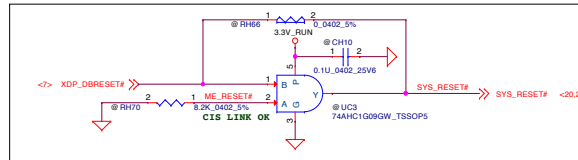


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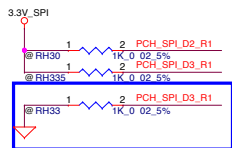
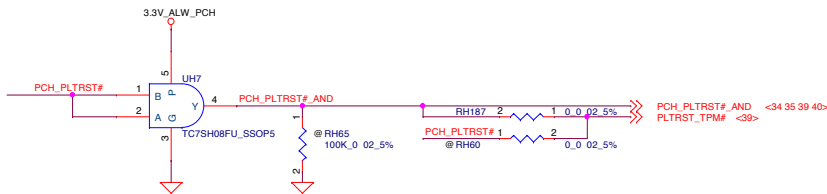
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KABYLAKE PCH-H (1/9)

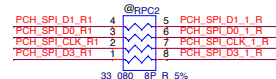
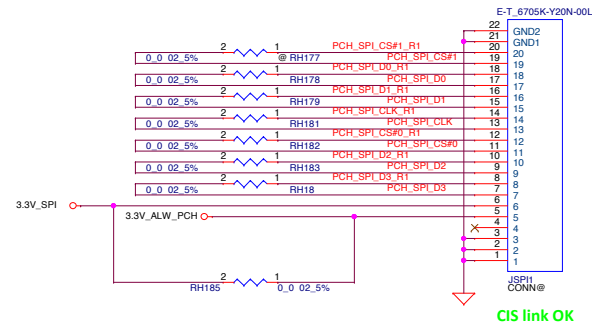
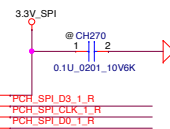
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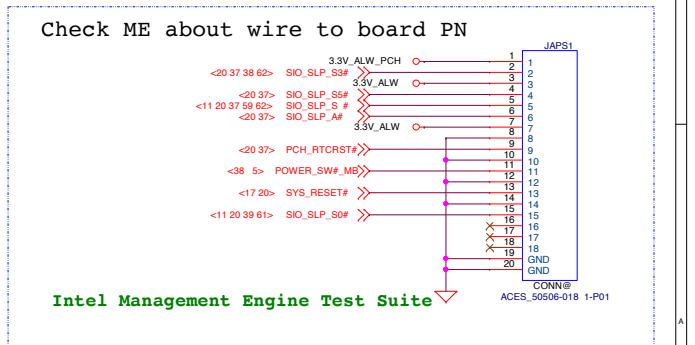
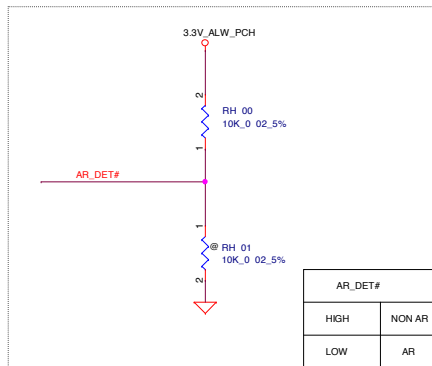
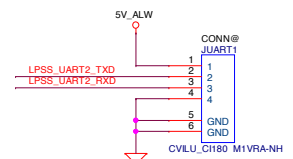
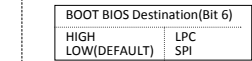
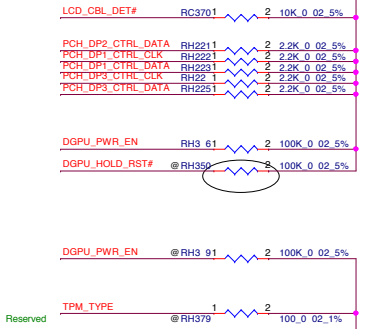


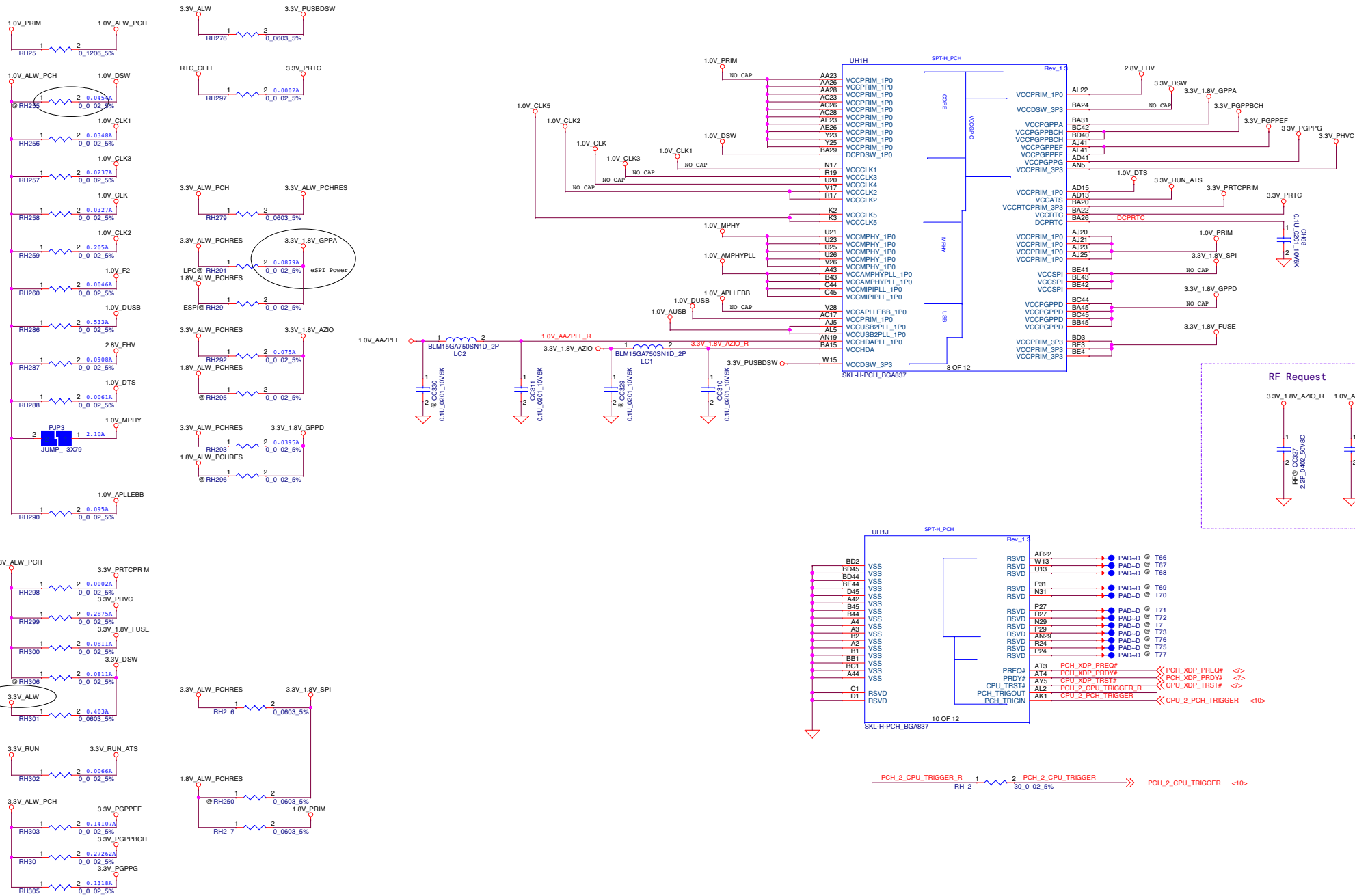
Note that the pull down resistor on SPI0\_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

Need check

|                                 |                             |     |  |
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| Size<br>B                       | Document Number             | Rev |  |
|                                 | <b>LA-E153P</b>             | 0.2 |  |







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|   |            |                 |            |                    |  | Date: Tuesday, June 28, 2016 | Sheet 22 of 7   |

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**Compal Electronics, Inc.**  
**KABYLAKE PCH-H (7/9)**





UH11 SPT-H\_PCH Rev. 1.3

|      |     |      |
|------|-----|------|
| AC18 | VSS | AR5  |
| AN4  | VSS | AR7  |
| AN10 | VSS | U15  |
| BE14 | VSS | AL4  |
| BE18 | VSS | AE29 |
| BE23 | VSS | AE4  |
| BE28 | VSS | AE42 |
| BE32 | VSS | AF18 |
| BE37 | VSS | AF20 |
| BE40 | VSS | AF21 |
| BE9  | VSS | AF23 |
| C10  | VSS | AF25 |
| C2   | VSS | AF26 |
| C28  | VSS | AF28 |
| C37  | VSS | AF29 |
| J7   | VSS | AG11 |
| K10  | VSS | AG13 |
| K27  | VSS | AG31 |
| K33  | VSS | AG32 |
| K36  | VSS | AG33 |
| K4   | VSS | AG38 |
| K42  | VSS | AG4  |
| K43  | VSS | AH1  |
| L12  | VSS | AH17 |
| L13  | VSS | AH18 |
| L15  | VSS | AH20 |
| L4   | VSS | AH21 |
| L41  | VSS | AH23 |
| L8   | VSS | AH25 |
| M35  | VSS | AH26 |
| M42  | VSS | AH28 |
| N10  | VSS | AH29 |
| N15  | VSS | AH45 |
| N19  | VSS | AJ10 |
| N22  | VSS | AJ14 |
| N24  | VSS | AJ15 |
| N35  | VSS | AJ17 |
| N36  | VSS | AJ18 |
| N4   | VSS | AJ26 |
| NM1  | VSS | AJ28 |
| N5   | VSS | AJ29 |
| P17  | VSS | AJ31 |
| P19  | VSS | AJ32 |
| P22  | VSS | AJ36 |
| P45  | VSS | AK4  |
| R10  | VSS | AK42 |
| R14  | VSS | AL7  |
| R22  | VSS | AV17 |
| R29  | VSS | AV24 |
| R33  | VSS | AV27 |
| R38  | VSS | AV21 |
| RS   | VSS | AV33 |
| T1   | VSS | AV6  |
| T2   | VSS | AW13 |
| T4   | VSS | AW19 |
| Y18  | VSS | AW29 |
| Y20  | VSS | AW37 |
| Y21  | VSS | AW9  |
| Y26  | VSS | AY38 |
| Y28  | VSS | A145 |
| Y29  | VSS | B25  |
| A18  | VSS | B3   |
| A25  | VSS | B37  |
| A32  | VSS | B40  |
| A37  | VSS | B6   |
| AA17 | VSS | BAT  |
| AA18 | VSS | BB11 |
| AA20 | VSS | BB18 |
| AA21 | VSS | BB21 |
| AA25 | VSS | BB25 |
| AA29 | VSS | BB30 |
| AA4  | VSS | BB34 |
| AA42 | VSS | Bc2  |
| AB10 | VSS | BD43 |
|      | VSS |      |

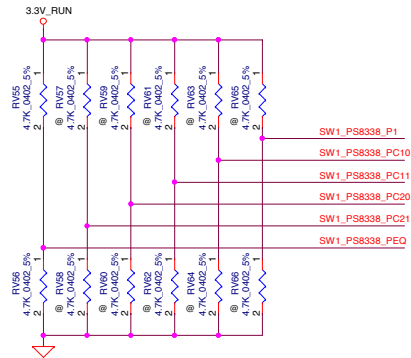
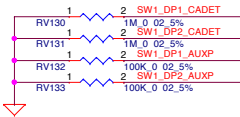
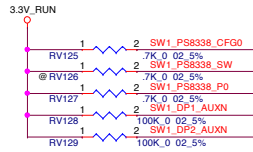
9 OF 12  
SKL-H-PCH\_BGA837

UH1L SPT-H\_PCH Rev. 1.3

|     |     |      |
|-----|-----|------|
| C42 | VSS | AB11 |
| D10 | VSS | AB7  |
| D12 | VSS | AB14 |
| D15 | VSS | AB31 |
| D16 | VSS | AB32 |
| D17 | VSS | AB38 |
| D19 | VSS | AB4  |
| D21 | VSS | AB5  |
| D24 | VSS | AC1  |
| D25 | VSS | AC20 |
| D27 | VSS | AC21 |
| D29 | VSS | AC25 |
| D30 | VSS | AC29 |
| D31 | VSS | AC45 |
| D33 | VSS | AB8  |
| D35 | VSS | AD11 |
| D36 | VSS | AD14 |
| E13 | VSS | AB15 |
| E15 | VSS | AD32 |
| E31 | VSS | AD33 |
| E33 | VSS | AD36 |
| F44 | VSS | AD4  |
| F8  | VSS | AD8  |
| G42 | VSS | AE18 |
| G9  | VSS | AE20 |
| H17 | VSS | AE21 |
| H19 | VSS | AE25 |
| H22 | VSS | AE28 |
| H24 | VSS | AL10 |
| H27 | VSS | AL11 |
| H29 | VSS | AL13 |
| H3  | VSS | AL17 |
| H35 | VSS | AL19 |
| J10 | VSS | AL24 |
| J11 | VSS | AL29 |
| J3  | VSS | AL32 |
| J39 | VSS | AL33 |
| J5  | VSS | AL38 |
| J42 | VSS | AM15 |
| U10 | VSS | AM17 |
| U11 | VSS | AM19 |
| U14 | VSS | AM22 |
| U17 | VSS | AM24 |
| U18 | VSS | AM27 |
| U28 | VSS | AM29 |
| U29 | VSS | AM45 |
| U31 | VSS | AN11 |
| U32 | VSS | AN22 |
| U33 | VSS | AN27 |
| U38 | VSS | AN31 |
| U4  | VSS | AN39 |
| U8  | VSS | AN7  |
| V18 | VSS | AN8  |
| V20 | VSS | AP11 |
| V21 | VSS | AP4  |
| V23 | VSS | AR33 |
| V25 | VSS | AR34 |
| V29 | VSS | AR42 |
| V3  | VSS | AR6  |
| V45 | VSS | AT10 |
| W14 | VSS | AT15 |
| W31 | VSS | AT36 |
| W32 | VSS | A19  |
| W33 | VSS | AU1  |
| W38 | VSS | AU35 |
| W4  | VSS | AU36 |
| W8  | VSS | AU39 |
| Y17 | VSS | AU45 |
|     | VSS | C4   |

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SKL-H-PCH\_BGA837

|   |  |  |  |                    |  |                               |  |
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|   |  |  |  | Sheet              |  | 2 of 7                        |  |
|   |  |  |  | Rev                |  | 0.2                           |  |

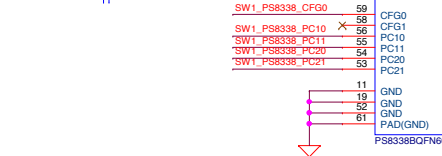
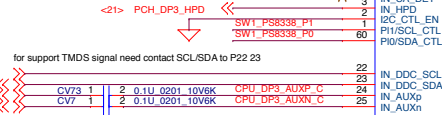
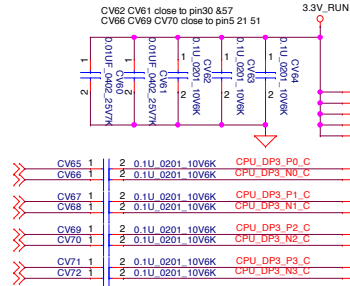


Port switching control or priority configuration Internal pull down -150K $\Omega$ , 3.3V I/O  
For Control Switching Mode (CFG0 = L)  
SW = L Port1 is selected (default)  
SW = H Port2 is selected  
For Automatic Switching Mode (CFG0 = H)  
SW = L Port1 has higher priority when both ports are plugged (default)  
SW = H Port2 has higher priority when both ports are plugged

Vendor suggest MUX use LLEQ\_PEQ=M and P0=H !!

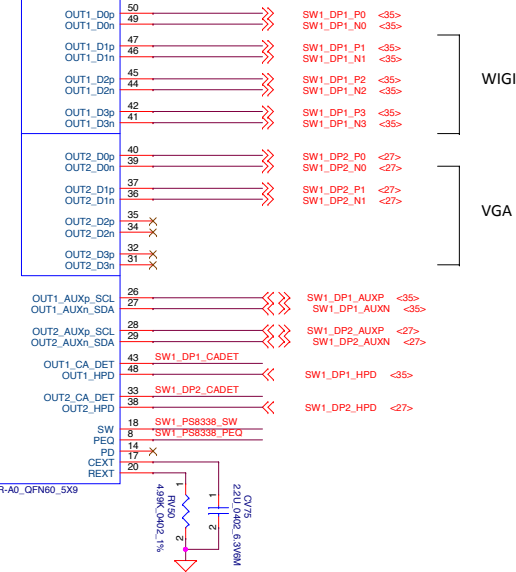
Programmable input equalization levels, Internal pull down at ~150Kohm, 3.3V I/O  
PEQ =  
L default, LEQ, compensate channel loss up to 11.5dB @HBR2  
H HEQ, compensate channel loss up to 14.5dB @HBR2  
M LLEQ, compensate channel loss up to 8.5dB @HBR2

P0: Automatic EQ disable Internal pull down -150K ohm 3.3V I/O  
P0 = L: Automatic EQ enable (default)  
P0 = H: Automatic EQ disable

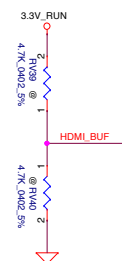
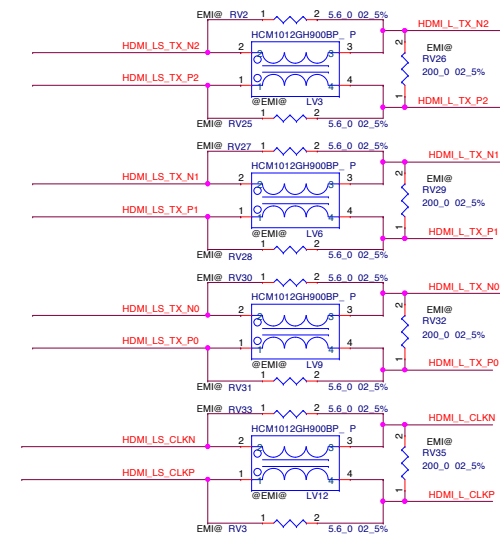
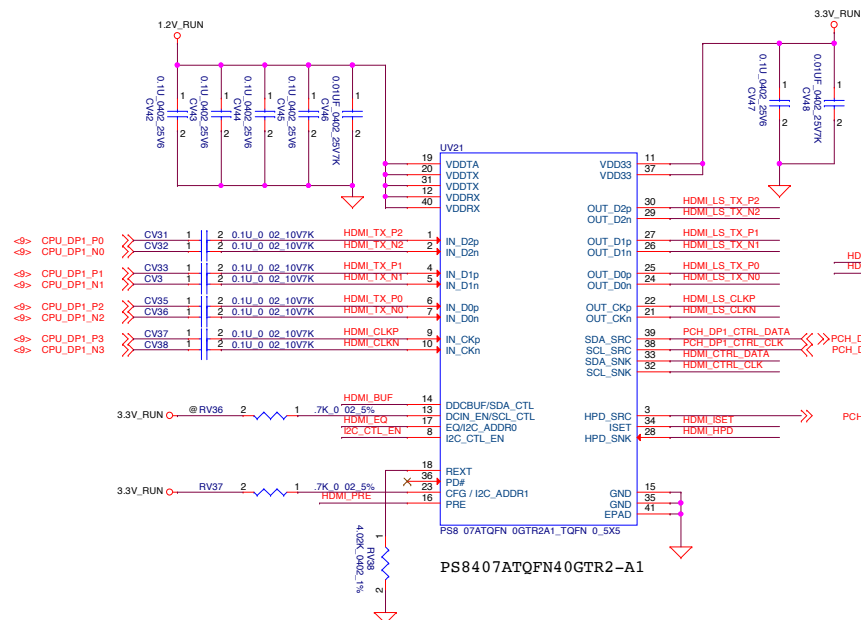


PS8338BQFN60GTR-A0\_QFN60\_5X9

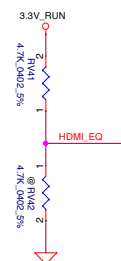
Priority : WIGI -> VGA



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| LA-E153P  |  |  |  | Date: Tuesday, June 28, 2016 |  |  |  | Sheet 25 of 7                 |  |  |  |

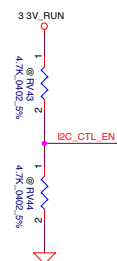


Enable active DDC buffer; internal pull down at ~150KΩ, 3.3V I/O  
 L passive DDC pass-through(default)  
 H active DDC buffer with default threshold  
 M active DDC buffer without internal pull up resistor



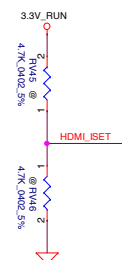
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.

- L programmable EQ for channel loss up to 12.4dB(default)
- H programmable EQ for channel loss up to 4.3dB
- M programmable EQ for channel loss up to 8.6dB

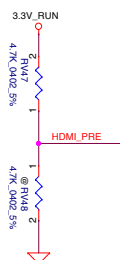


I2C Control enable Internal pull down at 150k 3.3V I/O

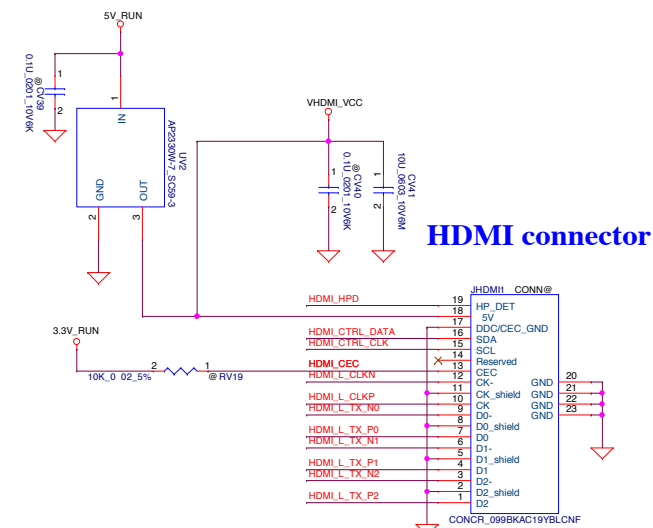
- L Pin control is selected with auto jitter cleaning (default)
- H I2C control is selected with default I2C address
- M Pin control is selected with full jitter cleaning



TMDS output swing adjustment; internal pull down at  $\sim 150k\Omega$ , 3.3V I/O.  
L default, 1000mV  
H increase +13%  
M reduce -13%



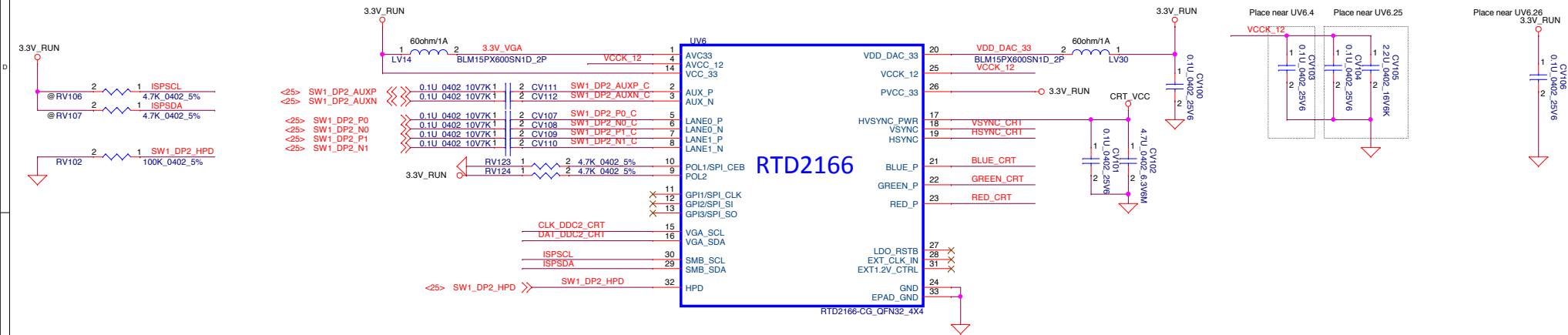
Output pre-emphasis setting: Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
 L no pre-emphasis(default)  
 H 1.6dB pre-emphasis  
 M 2.5dB pre-emphasis



|   |  |                    |                 |  |   |
|---|--|--------------------|-----------------|--|---|
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|   |  |                    |                 | Size                                       | Document Number<br><b>LA-EI53P</b>            |
|   |  |                    |                 | Date:                                      | Tuesday, June 28, 2016                        |
|   |  |                    |                 | Sheet                                      | 26 of 7                                       |

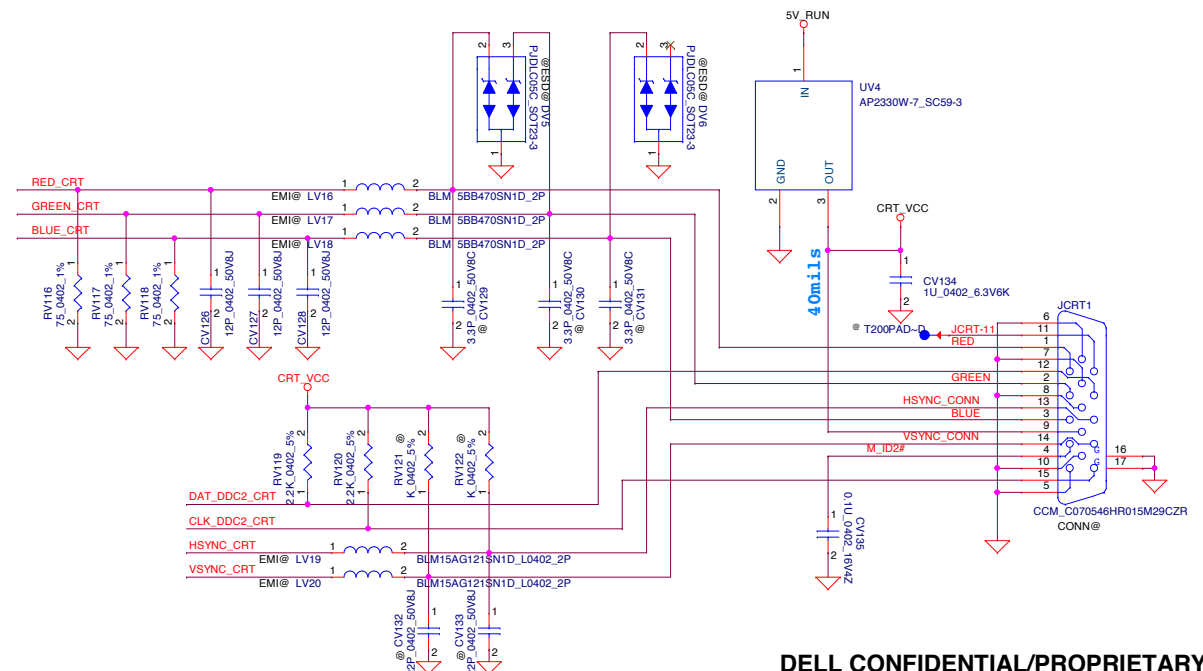
For TBT SW2\_DP2  
For non-TBT SW1\_DP2

## For Realtek Solution



### Operation Mode Table

|              |   | POL1(P10) |        |
|--------------|---|-----------|--------|
|              |   | 0         | 1      |
| POL2<br>(P9) | 0 | X         | X      |
|              | 1 | ROM       | EEPROM |



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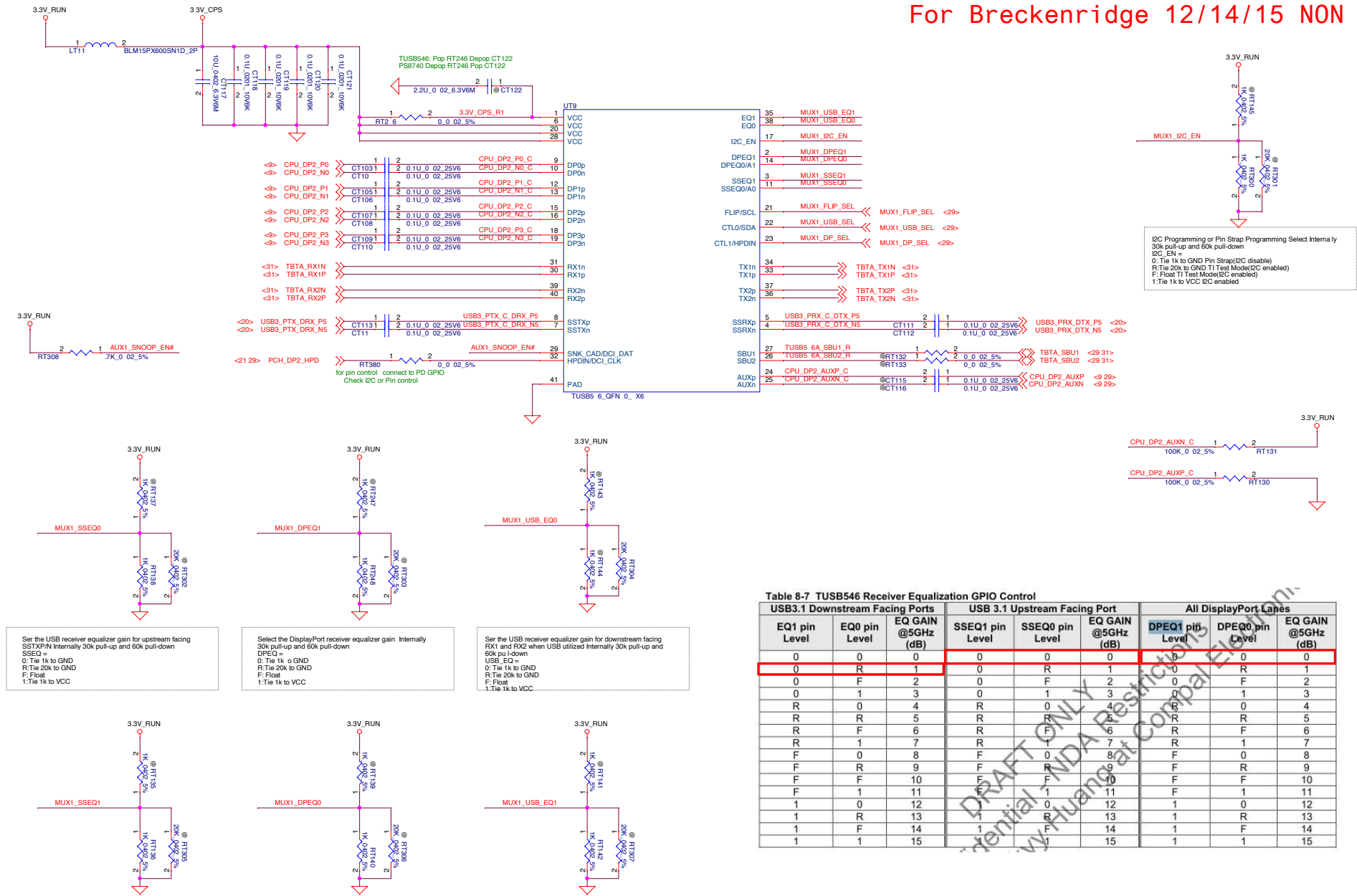
### ***DP to VGA & VGA Conn***

Document Number  
**LA-E153P**

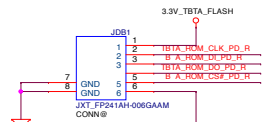
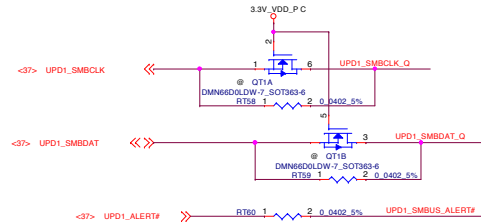
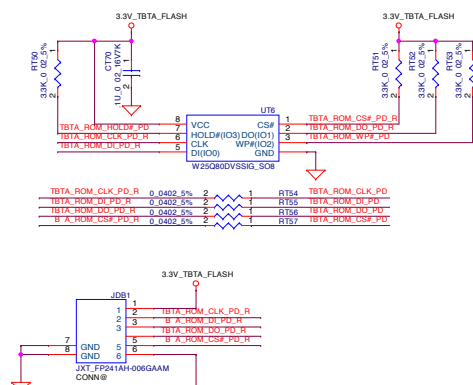
|     |     |
|-----|-----|
| Rev | 0.2 |
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|      |                      |       |    |    |    |
|------|----------------------|-------|----|----|----|
| Date | Tuesday June 28 2016 | Sheet | 27 | of | 74 |
|------|----------------------|-------|----|----|----|

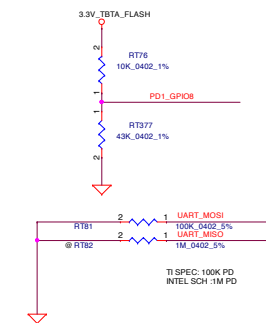
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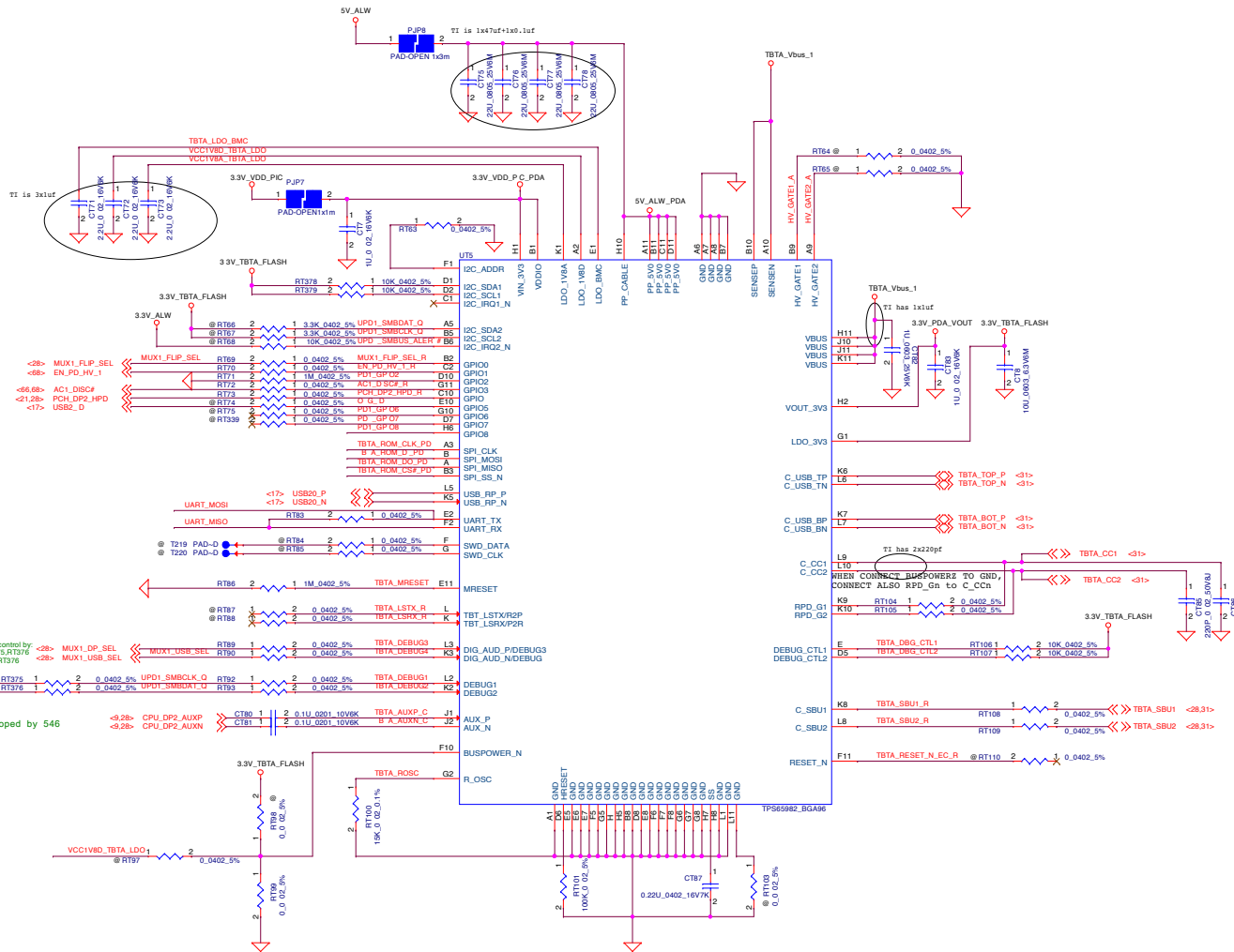
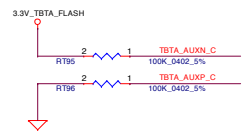
For Non-AR config



| DIV = R2 / (R1+R2) |         | Factory Device Configuration | Description  |
|--------------------|---------|------------------------------|--|
| DIV_min            | DIV_max |                              |  |
| 0.00               | 0.08    | 0                            | UFP only<br>5V @0.9A Sink capability with Ask for Max/ or anything from 0.9-3.0A<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes not supported<br>TV D supported  |
| 0.10               | 0.18    | 1                            | UFP only<br>5V @0.9A Sink capability with Ask for Max/ or anything from 0.9-3.0A<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes -Sink, C and D pin configuration<br>TV D supported   |
| 0.20               | 0.28    | 2                            | UFP only<br>5V @3.0A Sou ce capability<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes not supported<br>TV D supported  |
| 0.30               | 0.38    | 3                            | UFP only<br>5V @3.0A Sou ce capability<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes -Sink, C and D pin configuration<br>TV D supported   |
| 0.40               | 0.48    | 4                            | DRP<br>5V @0.9-3.0A Sink capability<br>5V @3.0A Sou ce capability<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes not supported<br>TV D supported<br>Accepts data and power role swaps, but does not initiate                 |
| 0.50               | 0.58    | 5                            | DRP<br>5V @0.9-3.0A Sink capability<br>5V @3.0A Sou ce capability<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes - Source, C, D, and E pin configuration<br>TV D supported<br>Accepts power role swaps but will not initiate |
| 0.60               | 0.68    | 6                            | DRP<br>5V @0.9-3.0A Sink capability<br>5V @3.0A Sou ce capability<br>TBT A terminate Modes not supported<br>D playPort Alternate Modes - Source, C, D, and E pin configuration<br>TV D supported<br>Accepts power role swaps but will not initiate |
| 0.70               | 1.00    | 7                            | Infinite boot retry from Flash to Host IF cycles.  |



Route in pass through manner so AUX can be snooped by 546



Need Link TPS65982D

DELL CONFIDENTIAL/PROPRIETARY

**Compal Electronics, Inc.**

**[Type C]PD Controller T**

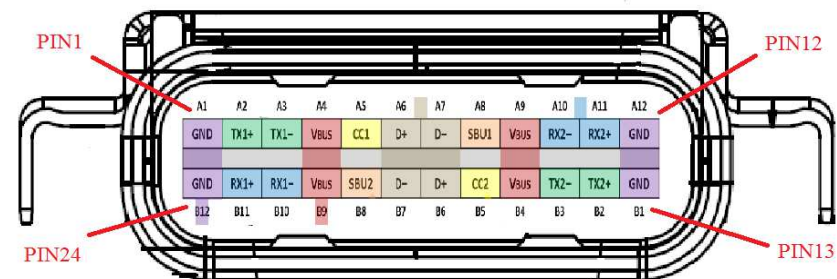
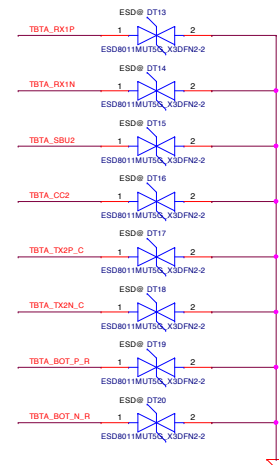
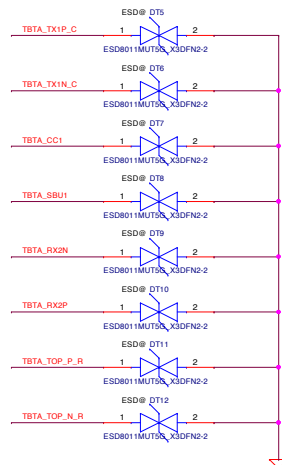
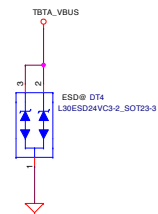
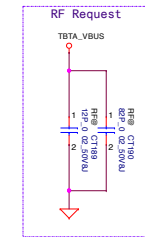
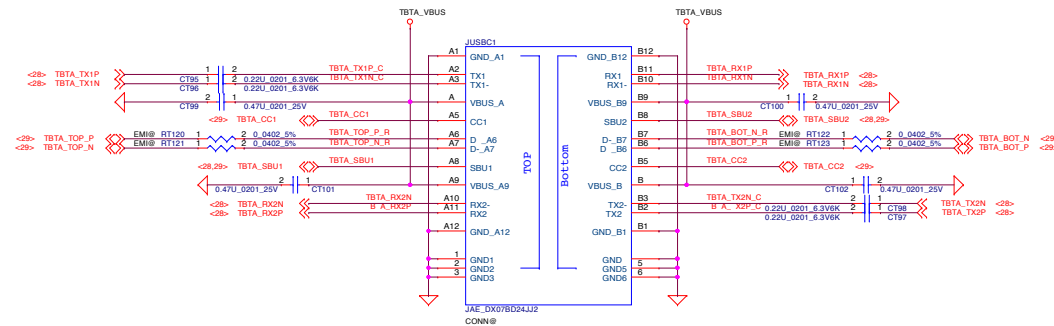
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| Security Classification  | Compal Secret Data |                 | TYPE CONFIDENTIAL NOT REPEAT       |   |
| Issued Date  | 2016/01/01         | Deciphered Date | 2017/01/01                         | <b>Compal Electronics, Inc.</b><br><b>[Type CPJD Controller TI]</b> |
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|           |                                    |            |
|-----------|------------------------------------|------------|
| Size<br>C | Document Number<br><b>LA-E153P</b> | Rev<br>0.2 |
|-----------|------------------------------------|------------|

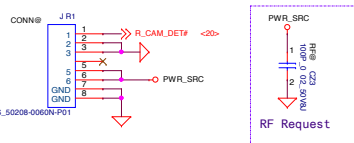
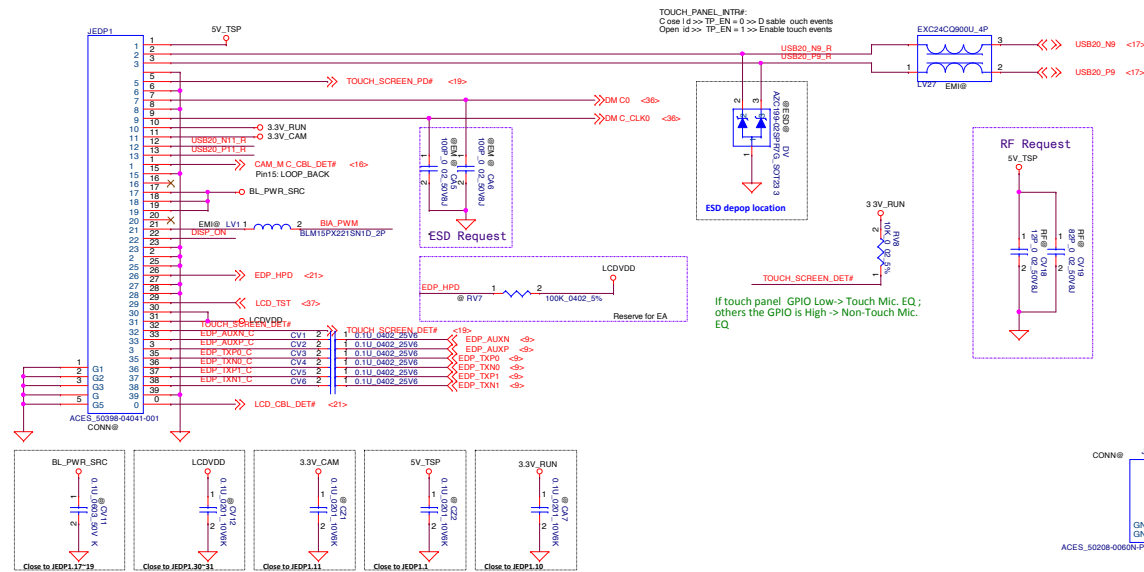




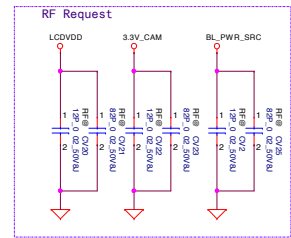
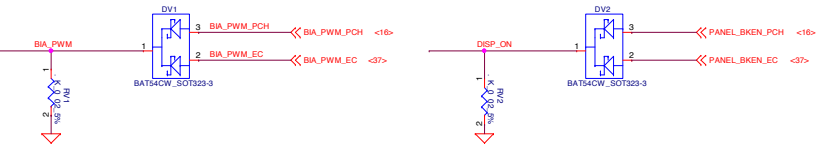
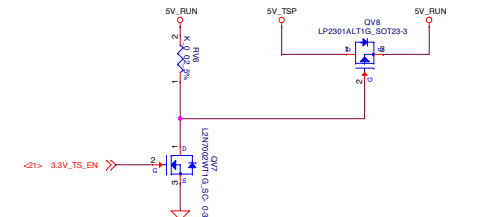
For NON AR Config



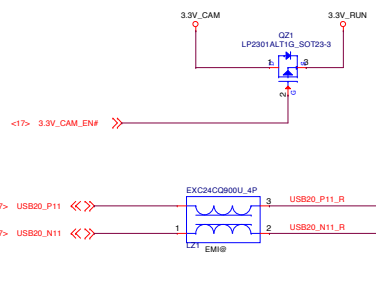
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| Issued Date  | 2016/01/01             | Deciphered Date    | 2017/01/01 | Title  | Size       |
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| Date:  | Tuesday, June 28, 2016 |                    | Sheet      | 31 of 74   |            |



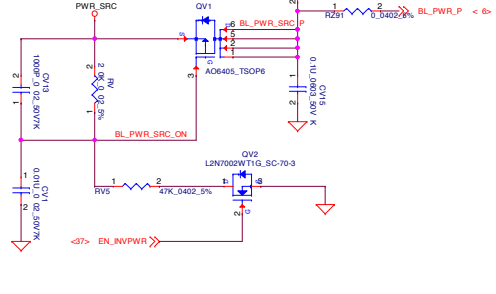
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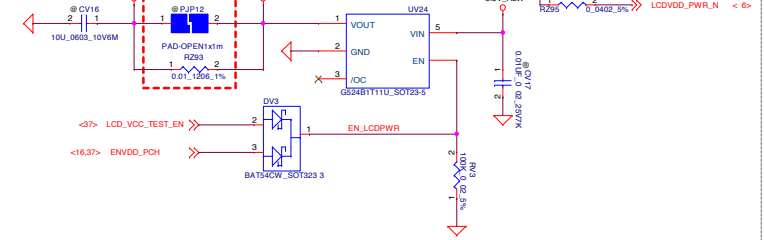
## WebCAM



## Backlight POWER



## LCDVDD POWER

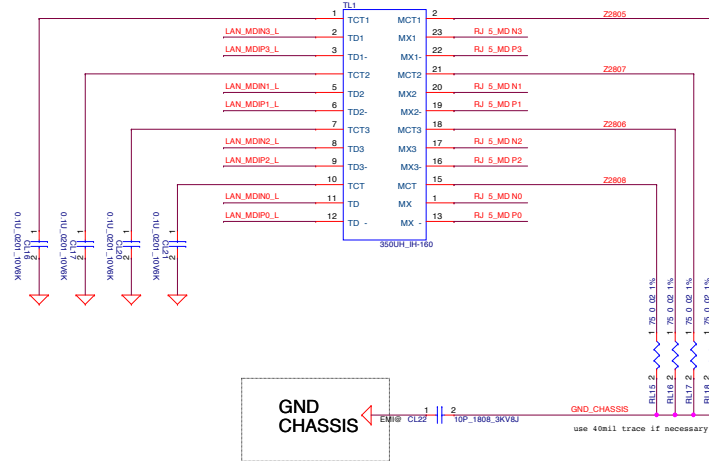
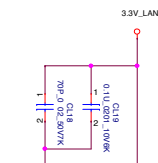
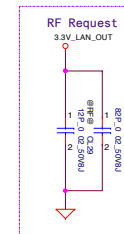


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

eDP CONN &amp; Touch screen

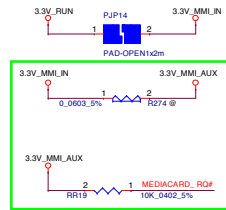
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| Issued Date   | 2016/01/01             | Deciphered Date | 2017/01/01 |
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| Date:   | Tuesday, June 28, 2016 | Sheet           | 32 of 74   |



GND  
CHASSIS

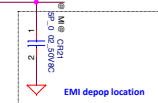
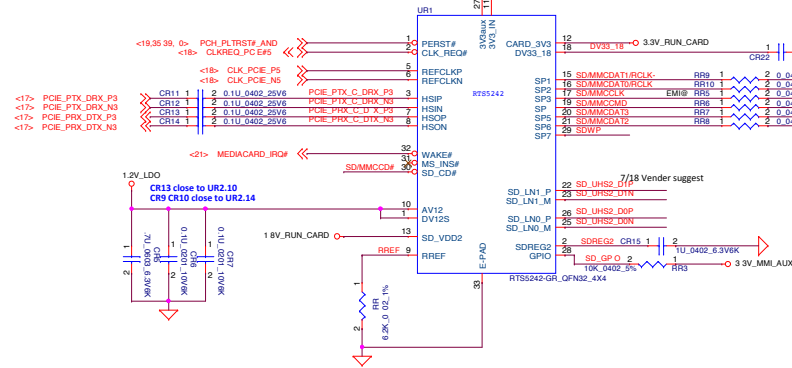
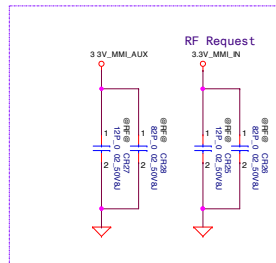
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|---|--------------------|-----------------|------------|---|----------|
| Security Classification   | Compel Secret Data |                 |            | Title   |          |
| Issued Date   | 2016/01/01         | Deciphered Date | 2017/01/01 | <b>Compel Electronics, Inc.</b><br><b>LAN Clarkville &amp; RJ45</b><br><b>Doc Number</b><br><b>LA-E153P</b> |          |
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| Date: <u>11/25/2016</u>   |                    |                 |            | Sheet   | 95 of 94 |

### For PCIe Interface

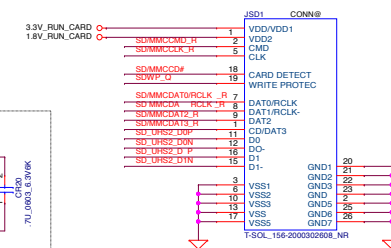
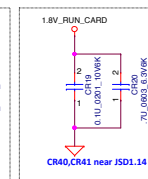
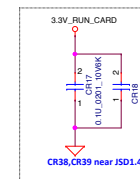
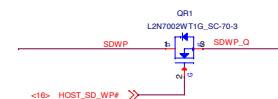


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

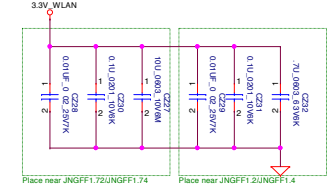
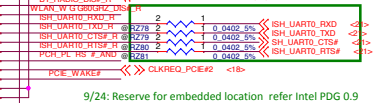
7/18 Vender suggest.



| HOST_SD_WP# | SDWP_Q | SDWP | STATUS                     |
|-------------|--------|------|----------------------------|
| High        | H gh   | High | Write Protect(SD LOCK)     |
|             | Low    | Low  | Write Enable               |
| Low         | H gh   | High | Write Protect(SD& FW LOCK) |
|             | Low    | High | Write Protect(FW LOCK)     |

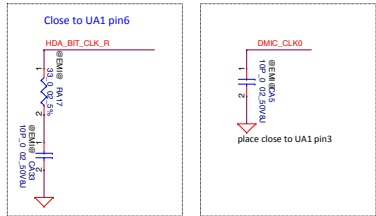
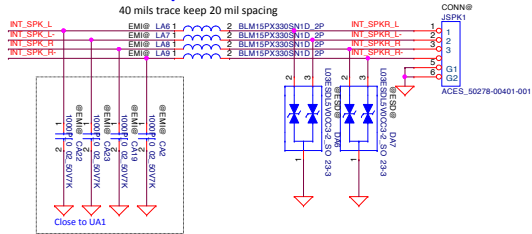


LINK SP070011U00 DONE

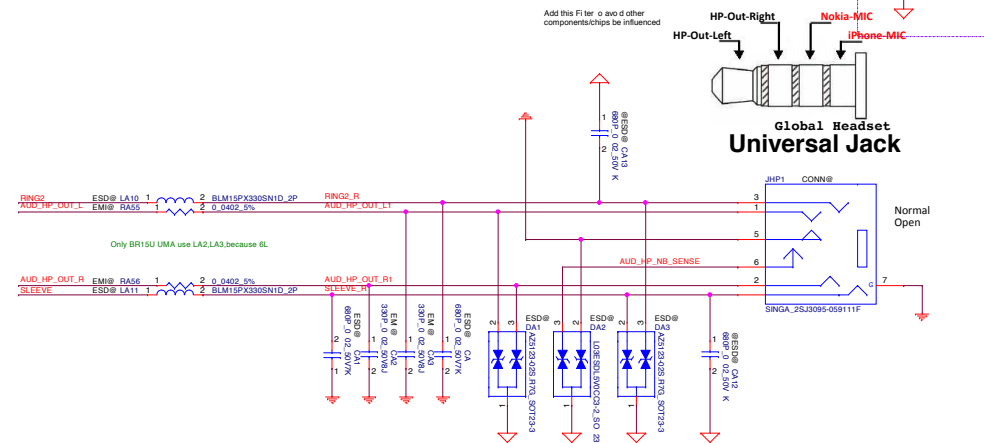
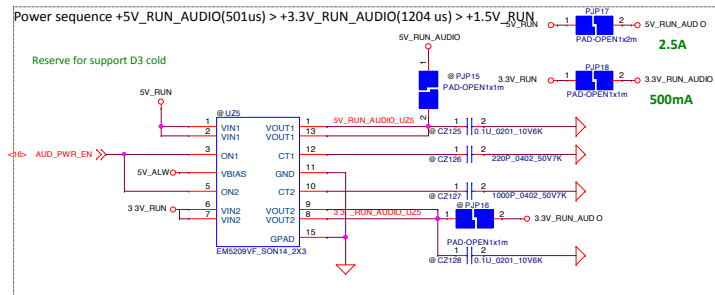
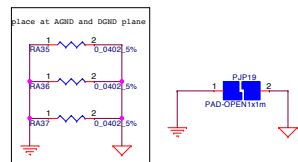
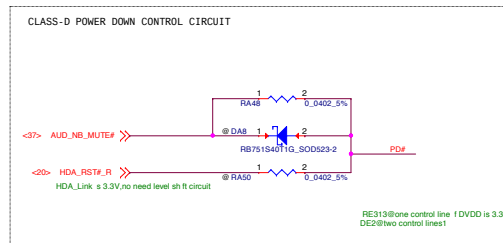
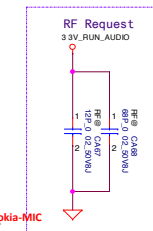
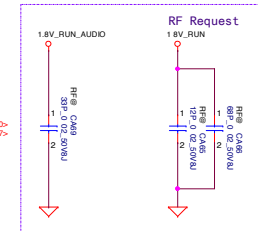
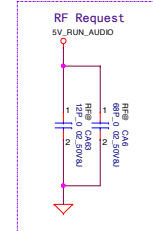
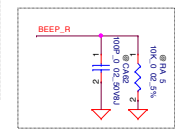
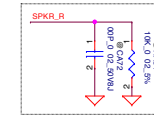
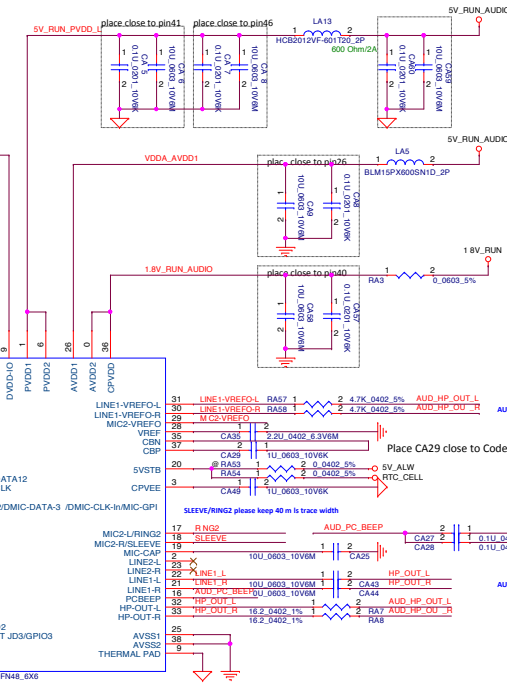
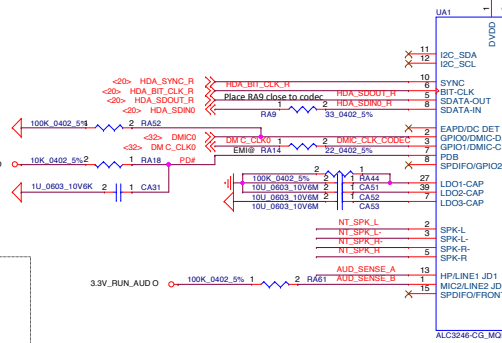
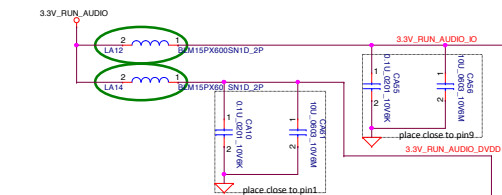
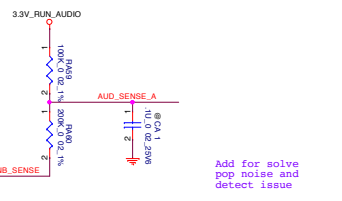


|       |    |    |            |
|-------|----|----|------------|
|       |    |    | Rev<br>0.2 |
| SHEET | 35 | of | 74         |

40 mils trace keep 20 mil spacing



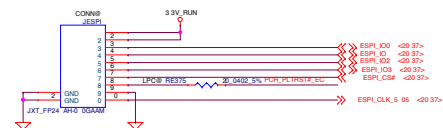
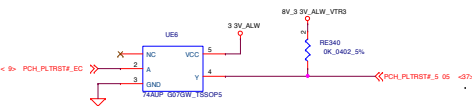
Place closely to Pin 13.



|  |  |  |                    |  |  |                      |  |  |
|--|--|--|--------------------|--|--|----------------------|--|--|
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| <p>Size</p>  |  |  |                    |  |  | <p>LA-E153P</p>      |  |  |

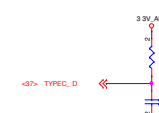
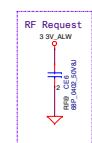
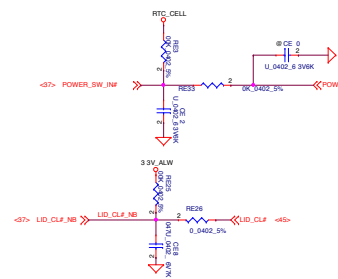




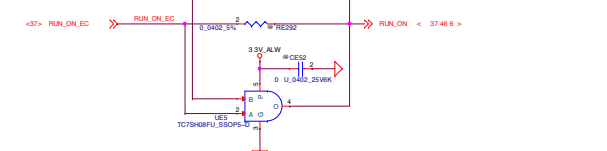
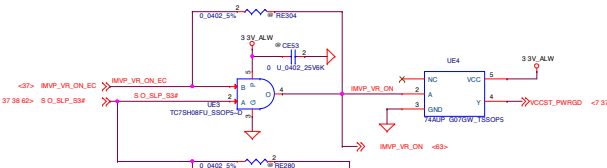


| LPC 80Port Debug | LPC         | ESPI      |
|------------------|-------------|-----------|
| 1                | +3 3V_RUN   | +3 3V_RUN |
| 2                | +3 3V_RUN   | +3 3V_RUN |
| 3                | LPC_LAD0    | ESPI_I00  |
| 4                | LPC_LAD1    | ESPI_I01  |
| 5                | LPC_LAD2    | ESPI_I02  |
| 6                | LPC_LAD3    | ESPI_I03  |
| 7                | LPC_FRAME#  | ESPI_CS#  |
| 8                | PCH_PLTRST# | NA        |
| 9                | GND         | GND       |
| 10               | LPC_CLOCK   | ESPI_CLK  |

| PAGE | ESPI               | LPC   |
|------|--------------------|---|
| 8    | RC25_10K           | RC8_15ohm<br>RC13/RC27_8.2K                   |
| 18   | RC212_0ohm<br>0603 | RC211_0ohm<br>0603                            |
| 31   |                    | RE337,RE338<br>RE339,RE340,<br>RE341<br>0_ohm |
| 32   | RE2 / RE3<br>0_ohm |   |



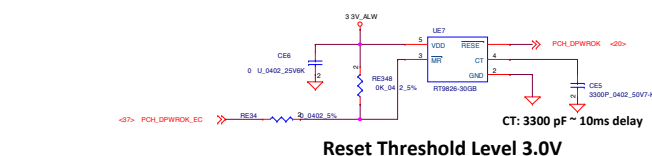
| RE343 | CE62  | REV                         |
|-------|-------|-----------------------------|
| 240K  | 4700p | Single Port ACE w/o AR      |
| 130K  | 4700p | Single Port ACE w/AR        |
| 62K   | 4700p | Dual Port ACE w/o AR        |
| 33K   | 4700p | Dual Port ACE w/AR          |
| 8.2K  | 4700p | Dual Port ACE (w/AR w/o AR) |
| 4.3K  | 4700p |                             |
| 2K    | 4700p |                             |
| 1K    | 4700p |                             |



| RE79 | CE40  | REV |
|------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p |     |
| 62K  | 4700p |     |
| 33K  | 4700p |     |
| 8.2K | 4700p |     |
| 4.3K | 4700p |     |
| 2K   | 4700p |     |
| 1K   | 4700p |     |

| RE300 | CE47  | PANEL SIZE |
|-------|-------|------------|
| 240K  | 4700p | 12"        |
| 130K  | 4700p | 14"        |
| 33K   | 4700p | BR15 H     |
| 4.3K  | 4700p | BR15 P     |

PD\_ACE\_DET# rise time is measured from 5% 68% BOARD\_ID rise time is measured from 5% 68% PANEL\_ID rise time is measured from 5% 68%

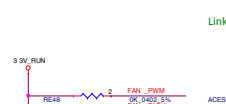
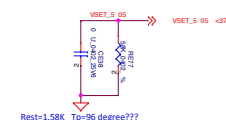
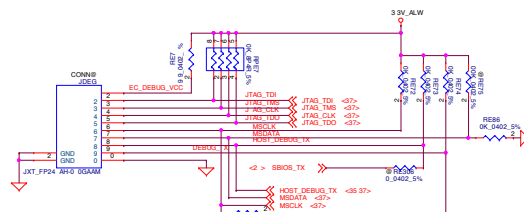
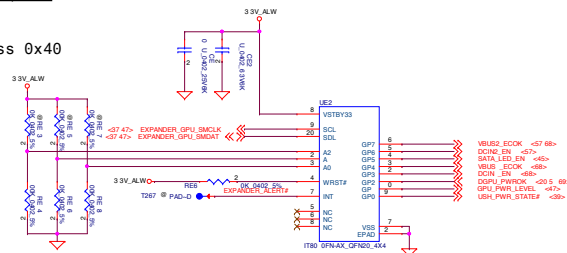


Reset Threshold Level 3.0V

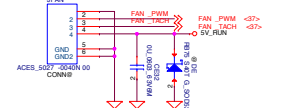
| Control Byte         |
|----------------------|
| 0 1 0 0 A2 A1 A0 R/H |

R/H = 0 = Wire  
R/H = 1 = Bond

SMBus address 0x40



Link 50271-0040N-001 DONE



Thermal diode mapping

| 5105 Channel | Location     |
|--------------|--------------|
| DP1/DN1      | CPU (QE3)    |
| DP2/DN2      | WiGig (QE5)  |
| DN2a/DP2a    | DDR (QE7)    |
| DP3/DN3      | NA           |
| DP4/DN4      | CPU VR (QE6) |

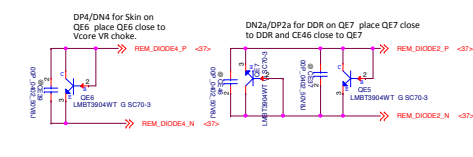
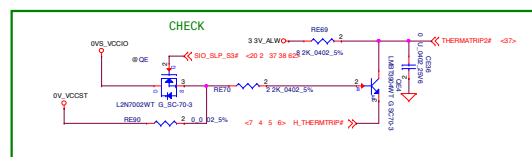
Place under CPU  
Place CE35 close to the QE3 as possible

Place under CPU  
Place CE35 close to the QE3 as possible

Place under CPU  
Place CE35 close to the QE3 as possible

Place under CPU  
Place CE35 close to the QE3 as possible

Place under CPU  
Place CE35 close to the QE3 as possible



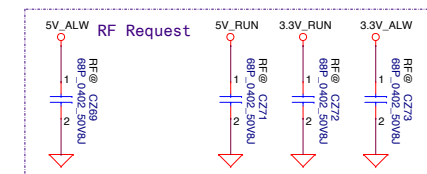
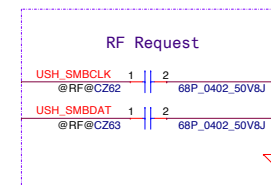
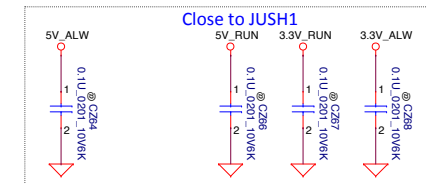
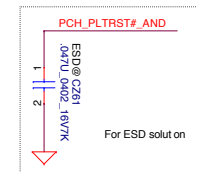
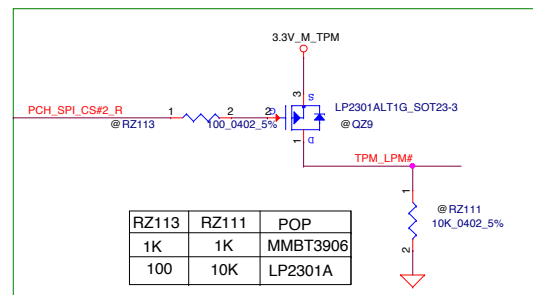
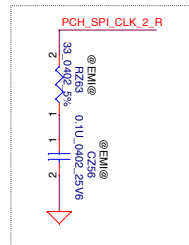
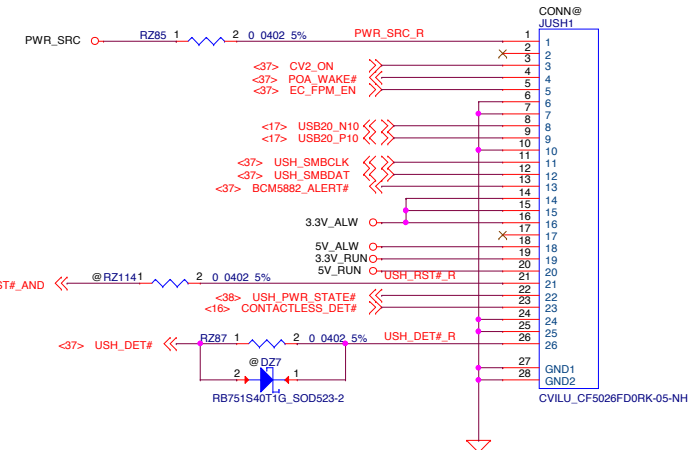
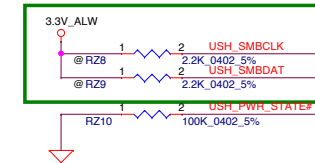
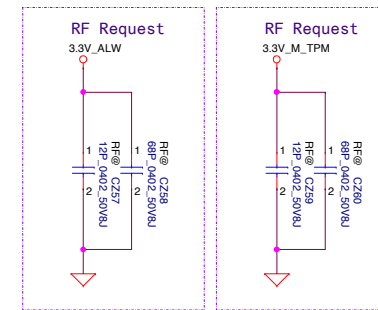
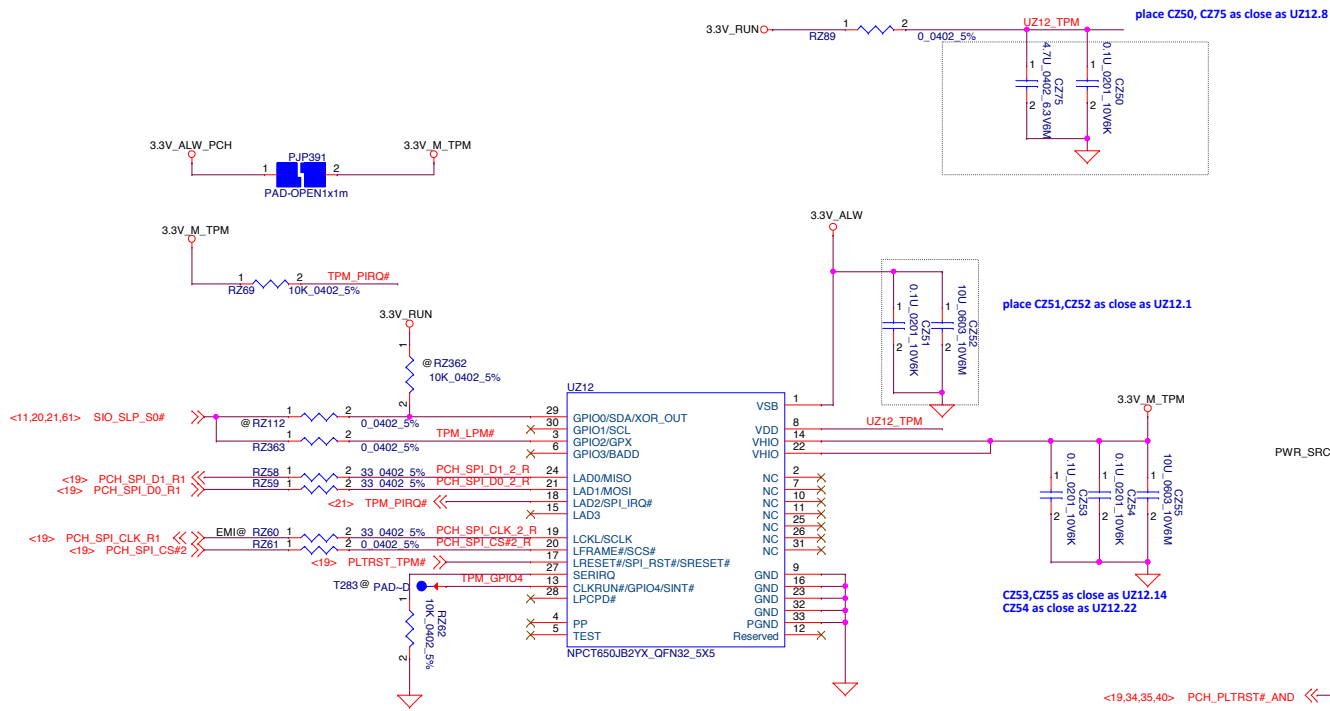
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MCS105 SUPPORT

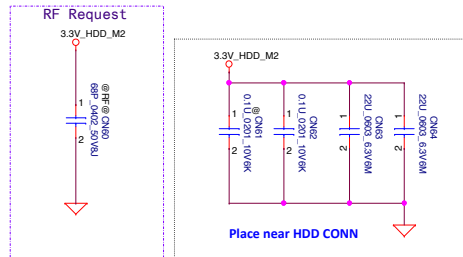
| Security Classification   | Compal Secret Data | Declassified Date | 110 |
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| Issued Date   | 2016/01/01         | 2017/01/01        |     |
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| Drawn   | LA-E153P           | Check Date        | 02  |

For NUVOTON TPM



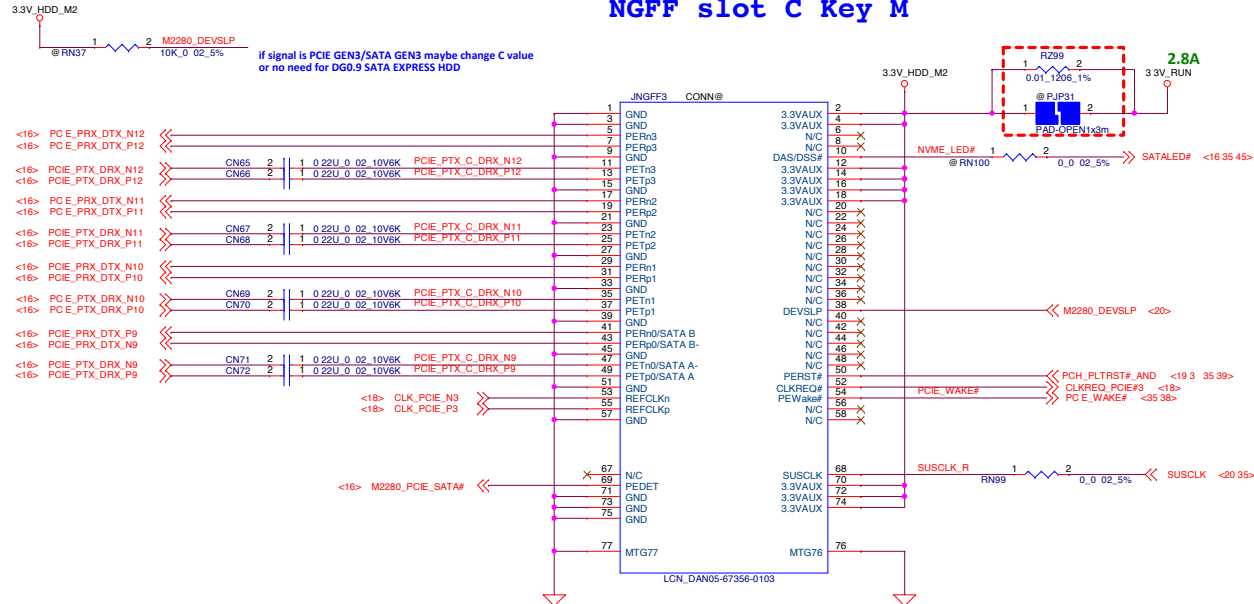
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| Security Classification   |                       | Compal Secret Data |            | <del>DECLASSIFIED</del><br><b>Compal Electronics, Inc.</b> |                      |
| Issued Date   | 2016/01/01            | Deciphered Date    | 2017/01/01 | Title  | <b>USH &amp; TPM</b> |
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|   |                       |                    |            | Document Number<br><b>LA-E153P</b>                         |                      |
| Date  | Thursday June 30 2016 |                    | Sheet      | 39   | of 74                |

For Breckenridge 15



2280 SSD

NGFF slot C Key M



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**Compal Electronics, Inc.**

## M2 2280 Socket

Document Number  
**LA-E153P**

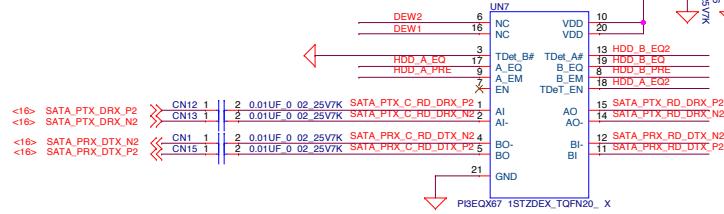
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|-------|------------------------|-------|---|----|---|
| Date: | Tuesday, June 28, 2016 | Sheet | 0 | of | 7 |
|-------|------------------------|-------|---|----|---|

|  |                    |                 |            |
|--|--------------------|-----------------|------------|
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**WWW.AliSaler.Com**

|         | pin 3   | pin 6 | pin 13  | pin 16 | pin 18  |
|---------|---------|-------|---------|--------|---------|
| Pericom | TDeT_B# | NC    | TDeT_A# | NC     | TDeT_EN |
| TI      | GND     | DEW2  | GND     | DEW1   | GND     |
| Parade  | GND     | REXT  | B_EQ2   | DEW    | A_EQ2   |

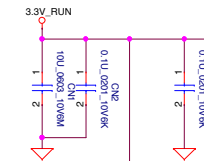
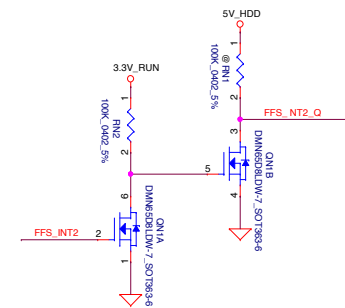
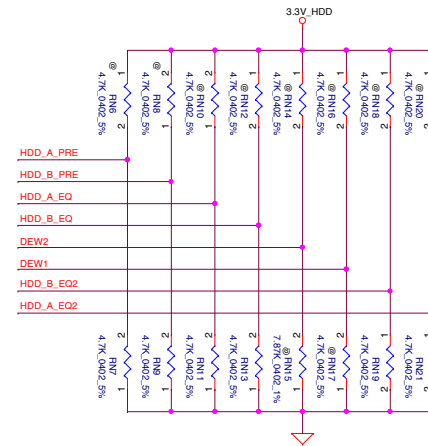
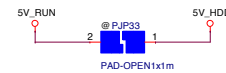
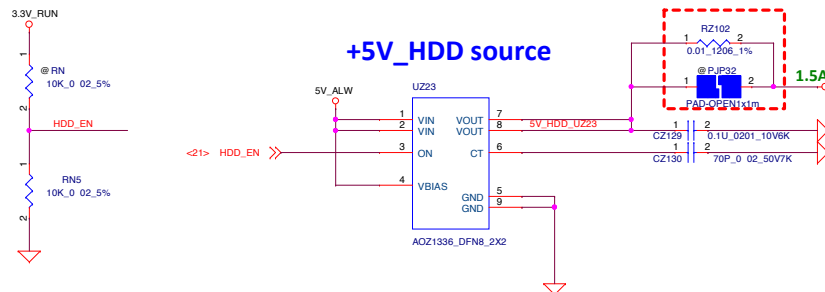
## SATA Repeater



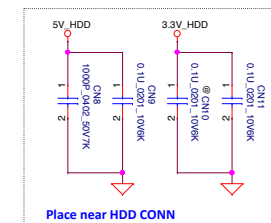
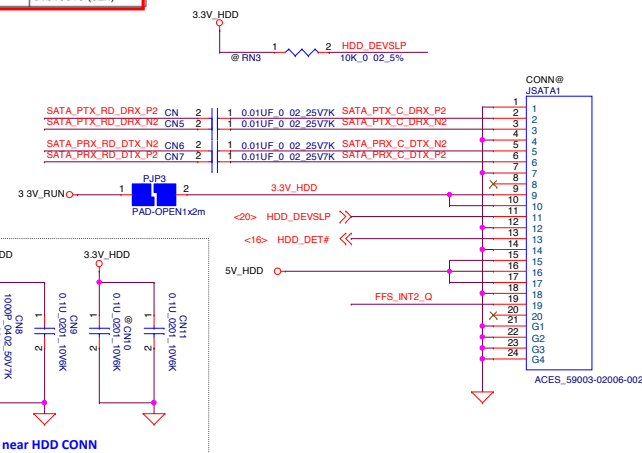
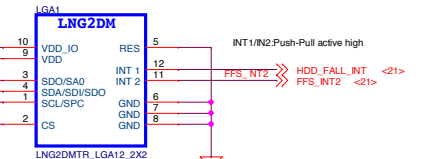
|                      | HDD_A_EQ<br>PIN17 | HDD_B_EQ<br>PIN19 | HDD_A_EQ2<br>PIN18 | HDD_B_EQ2<br>PIN13 | DEW1<br>PIN16   | DEW2<br>PIN6 | HDD_A_PRE<br>PIN9 | HDD_B_PRE<br>PIN8 |
|----------------------|-------------------|-------------------|--------------------|--------------------|-----------------|--------------|-------------------|-------------------|
| Pericom PI3EQX6741ST | PD<br>(RN13)      | PD<br>(RN16)      | PD<br>(RN83)       | PD<br>(RN23)       | NC              | NC           | PD<br>(RN5)       | PD<br>(RN11)      |
| TI SN75LVCP601       | PD<br>(RN13)      | NC                | PD<br>(RN83)       | PD<br>(RN23)       | NC<br>(IPU)     | NC<br>(IPU)  | PH<br>(RN8)       | PH<br>(RN10)      |
| Parade PS8527C       | PD<br>(RN13)      | PD<br>(RN16)      | PD<br>(RN83)       | PD<br>(RN23)       | NC<br>(1/2 VDD) | PD<br>(RN19) | NC<br>(1/2 VDD)   | NC<br>(1/2 VDD)   |

|      |         |   | A_EQ  | B_EQ  |        | A_EM                    | B_EM                    |
|------|---------|---|---|---|--------|-------------------------|-------------------------|
| Main | Pericom | 0<br>1  | 3dB<br>6dB<br>9dB   | 3dB<br>6dB<br>9dB   | 0<br>1 | 0dB<br>1.5dB            | 0dB<br>1.5dB            |
| 2nd  | TI      | 0<br>1  | 7dB<br>9dB<br>14dB  | 7dB<br>9dB<br>14dB  | 0<br>1 | 0dB<br>-4dB<br>-2dB     | 0dB<br>-4dB<br>-2dB     |
| 3rd  | Parade  | EQ2 EQ1<br>(M = VDD/2)<br>0 M<br>0 0<br>0 1<br>M M<br>M 0<br>M 1<br>1 M<br>1 0<br>1 1 | 2.4dB<br>7.4dB<br>14.4dB<br>12.2dB<br>9.4dB<br>13.3dB<br>6.2dB<br>11.2dB<br>5dB | 2.4dB<br>7.4dB<br>14.4dB<br>12.2dB<br>9.4dB<br>13.3dB<br>6.2dB<br>11.2dB<br>5dB | 0<br>1 | 0dB<br>-3.5dB<br>-1.5dB | 0dB<br>-3.5dB<br>-1.5dB |

\* red color is current setting



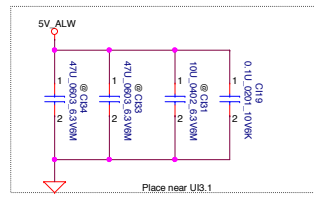
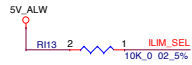
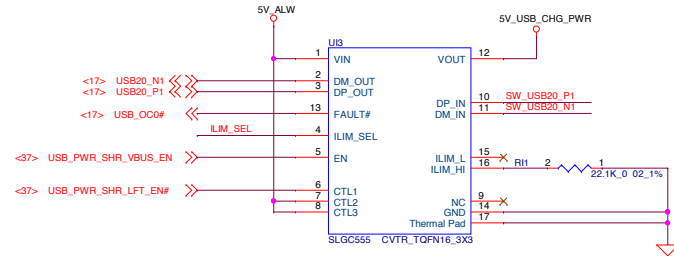
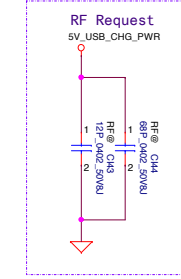
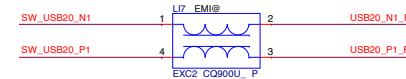
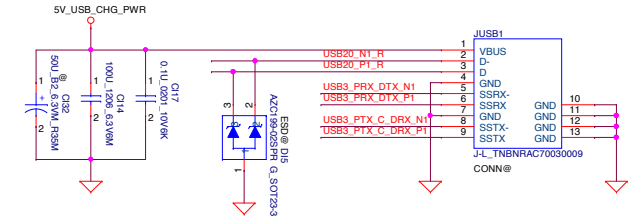
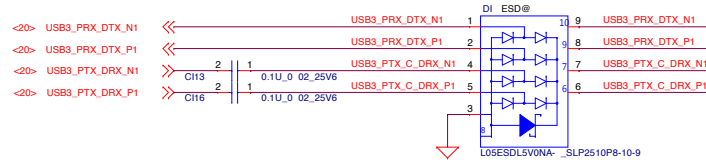
## Free Fall Sensor



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| Date: Tuesday, June 28, 2016  |  |  |  | Sheet              |                 | 1 of 7          |            |

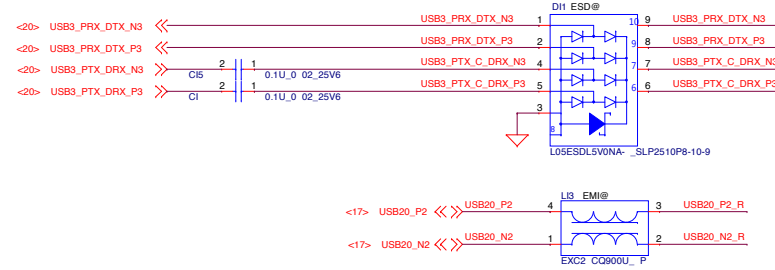
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Compal Electronics, Inc.

# For PWR SW + Charger combine IC

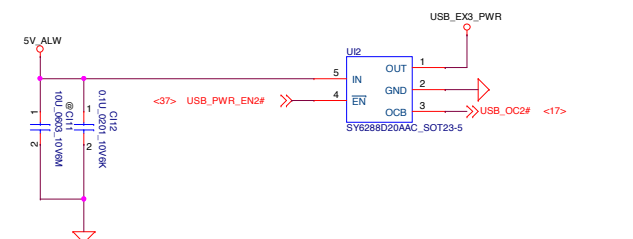
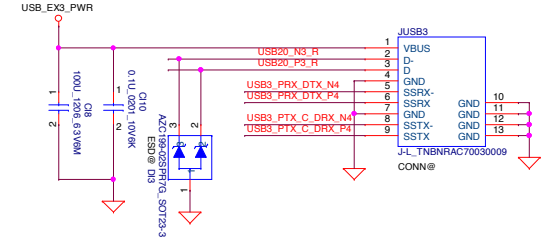
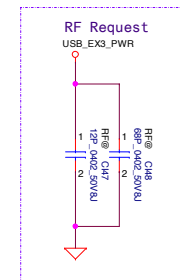
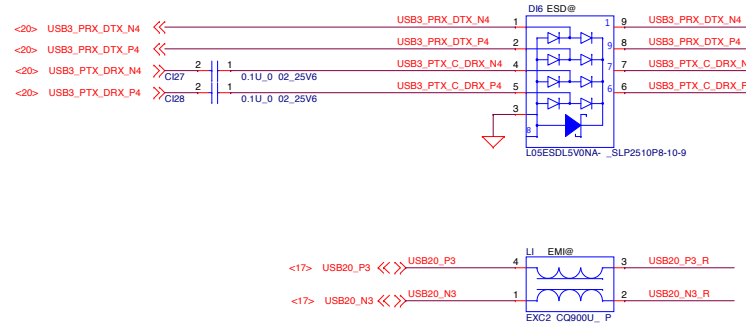
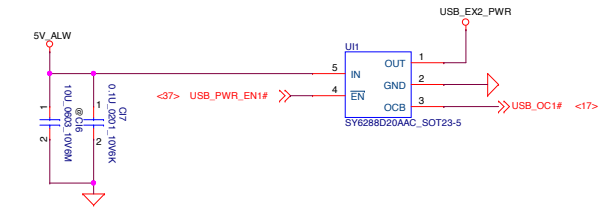
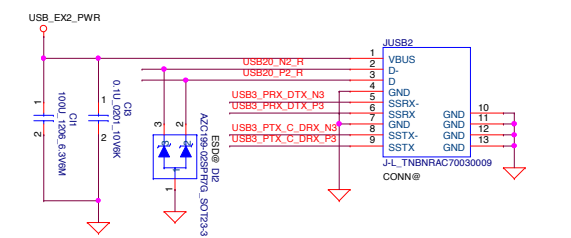
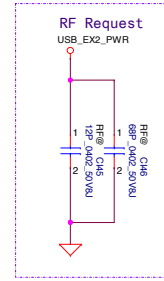


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| Size  |  | Document Number        |                 |   | Rev        |
| B   |  | LA-E153P               |                 |   | 0.2        |
| Date:   |  | Tuesday, June 28, 2016 |                 | Sheet 2 of 7  |            |

# For Breckenridge 14&15/Steamboat 14



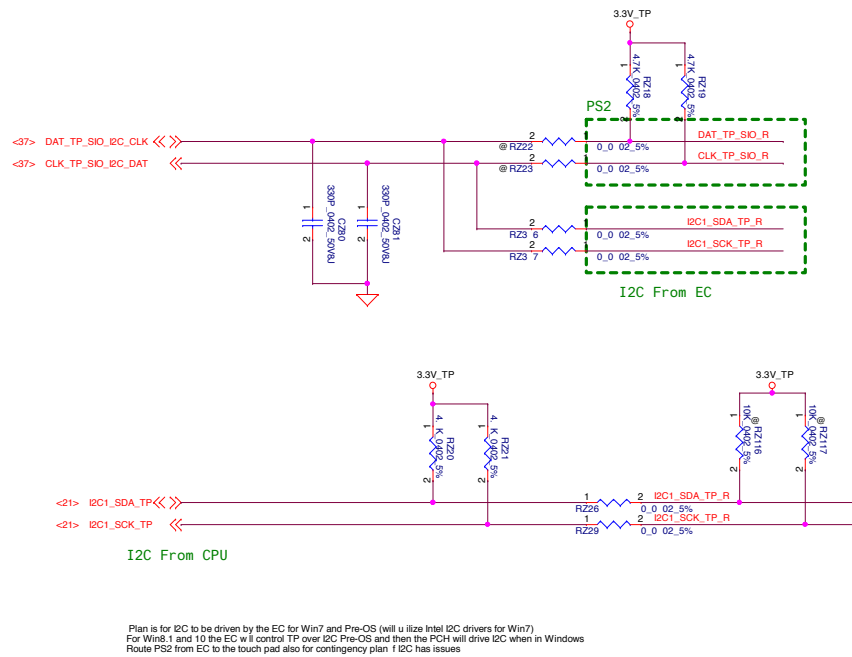
DfB request:  
main SM070003200 (INPAQ\_MCM1012B900F06BP\_4P)  
Footprint use 2nd source SM070004400 (PANAS\_EXC2CQ900U\_4P)  
Pitch change from 0.5mm to 0.55mm



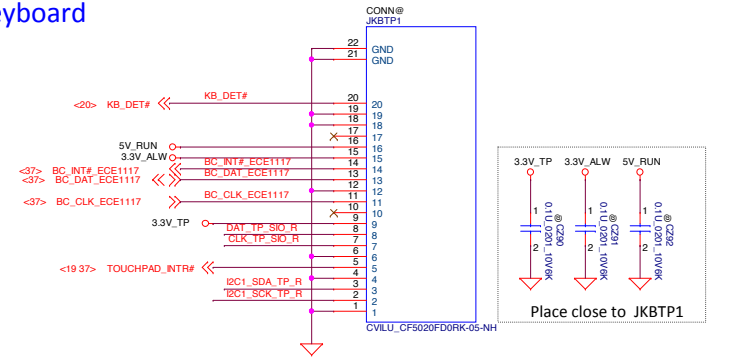
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| Security Classification   |  | Compal Secret Data |  | DELL CONFIDENTIAL/PROPRIETARY |  |                          |  |         |  |
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|   |  |                    |  |                               |  | JUSB2&JUSB3              |  |         |  |
|   |  |                    |  | Size B                        |  | Document Number          |  | Rev 0.2 |  |
|   |  |                    |  |                               |  | LA-E153P                 |  |         |  |
|   |  |                    |  | Date:                         |  | Tuesday, June 28, 2016   |  |         |  |
|   |  |                    |  | Sheet                         |  | 3 of 7                   |  |         |  |

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**Compal Electronics, Inc.**  
**JUSB2&JUSB3**

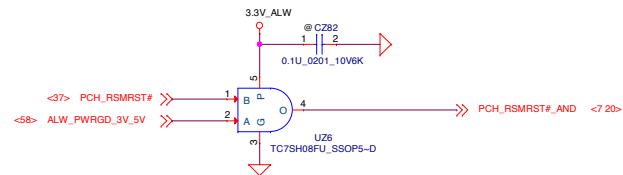
## Touch Pad



## Keyboard



## RSMRST circuit

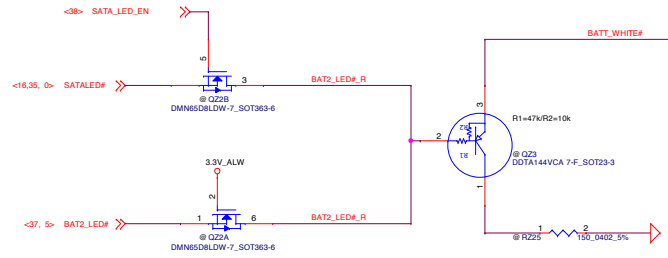


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| 2016/01/01  |  | 2017/01/01         |  | Keyboard                      |  |
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| LA-E153P  |  | 0.2                |  | Date: Tuesday, June 28, 2016  |  |
| Sheet   |  | of                 |  | 7                             |  |

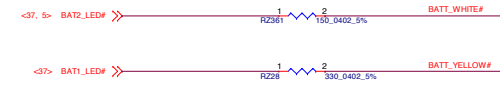


## HDD LED MUX

means EC can switch battery white led and HDD LED by hot key Fn H

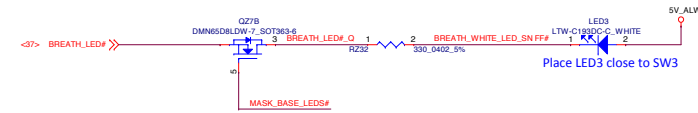


## Battery LED

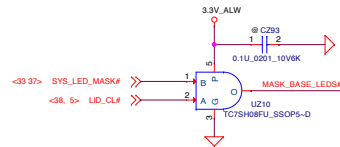


## Breath LED

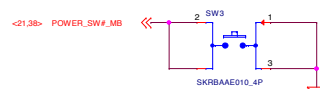
LED PIN change to SC50000FL00 from SC50000BA00



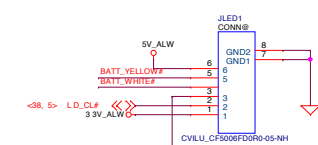
Place LED3 close to SW3



## POWER & INSTANT ON SWITCH



## LED board CONN

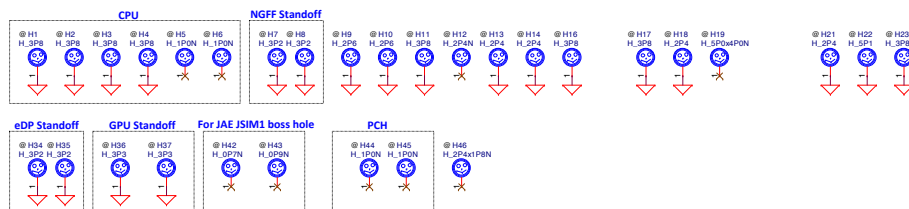


## Fiducial Mark

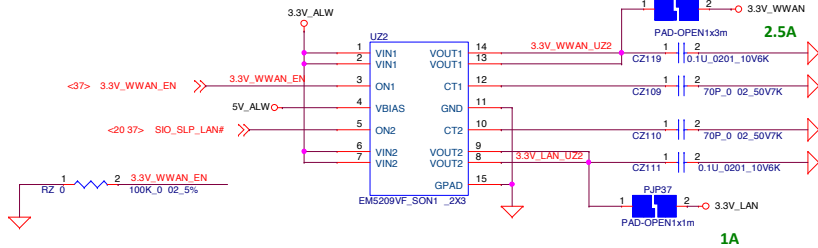


LED Circuit Control Table

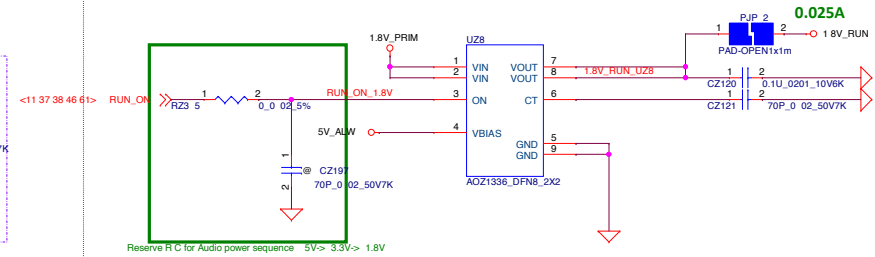
|                                  | SYS_LED_MASK# | LID_CL# |
|----------------------------------|---------------|---------|
| Mask All LEDs (Unobtrusive mode) | 0             | X       |
| Mask Base MB LEDs (Lid Closed)   | 1             | 0       |
| Do not Mask LEDs (Lid Opened)    | 1             | 1       |



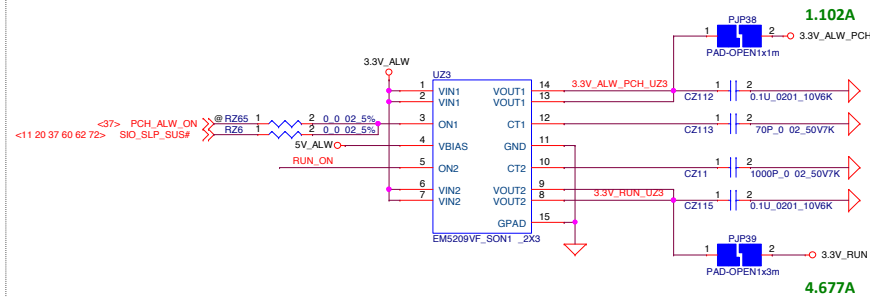
### +3.3V\_WWAN/+3.3V\_LAN source



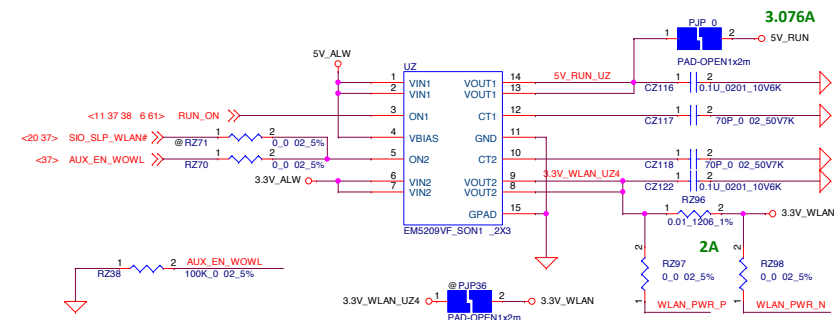
### +1.8V\_RUN source



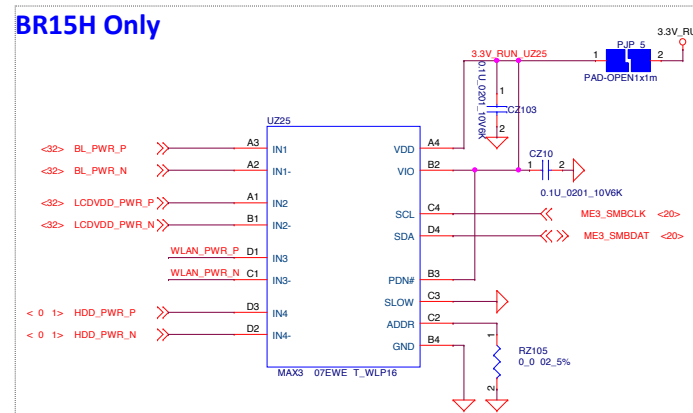
### +3.3V\_ALW\_PCH/+3.3V\_RUN source



### +5V\_RUN/+3.3V\_WLAN source



### BR15H Only



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Power control

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| Document Number   |                    |                 | Rev 0.2      |
| Date: Tuesday, June 28, 2016  |                    |                 | Sheet 6 of 7 |

|                          |                                      |
|--------------------------|--------------------------------------|
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| <B> PEG_CTX_C_GRX_N0_15] | >> PEG_CTX_C_GRX_N0_15]              |
| <B> PEG_CTX_C_GRX_P0_15] | >> PEG_CTX_C_GRX_P0_15]              |
| <B> PEG_CTX_C_GRX_N0_15] | >> PEG_CTX_C_GRX_N0_15]              |
| PEG_CRX_GTX_P0 CV 27 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P0  |
| PEG_CRX_GTX_N0 CV 28 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N0  |
| PEG_CRX_GTX_P1 CV 29 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P1  |
| PEG_CRX_GTX_N1 CV 30 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N1  |
| PEG_CRX_GTX_P2 CV 31 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P2  |
| PEG_CRX_GTX_N2 CV 32 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N2  |
| PEG_CRX_GTX_P3 CV 33 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P3  |
| PEG_CRX_GTX_N3 CV 3 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N3  |
| PEG_CRX_GTX_P CV 35 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P   |
| PEG_CRX_GTX_N CV 36 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N   |
| PEG_CRX_GTX_P5 CV 37 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P5  |
| PEG_CRX_GTX_N5 CV 38 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N5  |
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| PEG_CRX_GTX_N6 CV 2 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N6  |
| PEG_CRX_GTX_P7 CV 1 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P7  |
| PEG_CRX_GTX_N7 CV 2 2    | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N7  |
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| PEG_CRX_GTX_N10 CV 8 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N10 |
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| PEG_CRX_GTX_N13 CV 5 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N13 |
| PEG_CRX_GTX_P1 CV 55 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P1  |
| PEG_CRX_GTX_N1 CV 56 2   | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_N1  |
| PEG_CRX_GTX_P15 CV 57 2  | 1 0.22u 0 02 16V7K PEG_CRX_C_GTX_P15 |
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| PEG_CTX_C_GRX_N1 AN14  | PEG_RX1_N  |
| PEG_CTX_C_GRX_P2 AP14  | PEG_RX2    |
| PEG_CTX_C_GRX_N2 AP14  | PEG_RX2_N  |
| PEG_CTX_C_GRX_P3 AN15  | PEG_RX3    |
| PEG_CTX_C_GRX_N3 AN15  | PEG_RX3_N  |
| PEG_CTX_C_GRX_P4 AN17  | PEG_RX4    |
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| PEG_CTX_C_GRX_N6 AN18  | PEG_RX6_N  |
| PEG_CTX_C_GRX_P7 AN20  | PEG_RX7    |
| PEG_CTX_C_GRX_N7 AN20  | PEG_RX7_N  |
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| PEG_CTX_C_GRX_N11 AP23 | PEG_RX11_N |
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| PEG_CTX_C_GRX_N12 AN24 | PEG_RX12_N |
| PEG_CTX_C_GRX_P13 AN26 | PEG_RX13   |
| PEG_CTX_C_GRX_N13 AN26 | PEG_RX13_N |
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| PEG_CTX_C_GRX_N14 AP26 | PEG_RX14_N |
| PEG_CTX_C_GRX_P15 AN27 | PEG_RX15   |
| PEG_CTX_C_GRX_N15 AN27 | PEG_RX15_N |
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| PEG_CRX_C_GTX_N1 AG14  | PEG_TX1_N  |
| PEG_CRX_C_GTX_P2 AK15  | PEG_TX2    |
| PEG_CRX_C_GTX_N2 AJ15  | PEG_TX2_N  |
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| PEG_CRX_C_GTX_N3 AK16  | PEG_TX3_N  |
| PEG_CRX_C_GTX_P4 AK17  | PEG_TX4    |
| PEG_CRX_C_GTX_N4 AJ17  | PEG_TX4_N  |
| PEG_CRX_C_GTX_P5 AH17  | PEG_TX5    |
| PEG_CRX_C_GTX_N5 AG17  | PEG_TX5_N  |
| PEG_CRX_C_GTX_P6 AK18  | PEG_TX6    |
| PEG_CRX_C_GTX_N6 AJ18  | PEG_TX6_N  |
| PEG_CRX_C_GTX_P7 AK19  | PEG_TX7    |
| PEG_CRX_C_GTX_N7 AJ19  | PEG_TX7_N  |
| PEG_CRX_C_GTX_P8 AK20  | PEG_TX8    |
| PEG_CRX_C_GTX_N8 AJ20  | PEG_TX8_N  |
| PEG_CRX_C_GTX_P9 AH20  | PEG_TX9    |
| PEG_CRX_C_GTX_N9 AG20  | PEG_TX9_N  |
| PEG_CRX_C_GTX_P10 AK21 | PEG_TX10   |
| PEG_CRX_C_GTX_N10 AJ21 | PEG_TX10_N |
| PEG_CRX_C_GTX_P11 AL22 | PEG_TX11   |
| PEG_CRX_C_GTX_N11 AK22 | PEG_TX11_N |
| PEG_CRX_C_GTX_P12 AK23 | PEG_TX12   |
| PEG_CRX_C_GTX_N12 AJ23 | PEG_TX12_N |
| PEG_CRX_C_GTX_P13 AH23 | PEG_TX13   |
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| PEG_CRX_C_GTX_P14 AK24 | PEG_TX14   |
| PEG_CRX_C_GTX_N14 AJ24 | PEG_TX14_N |
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Part 1 of 7

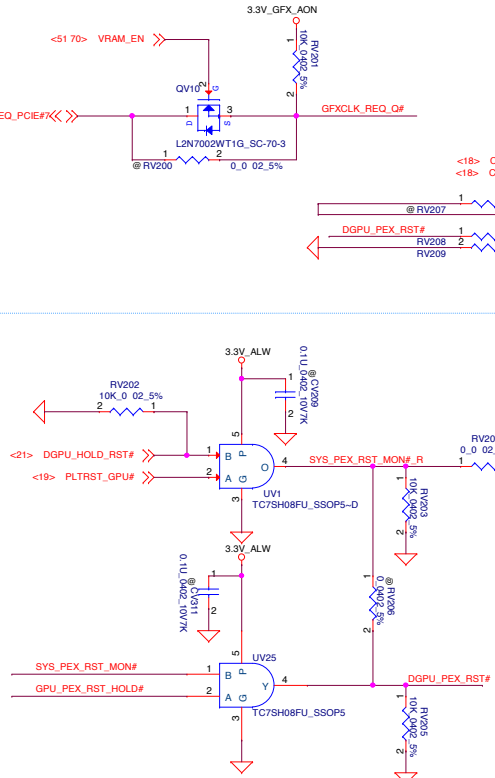
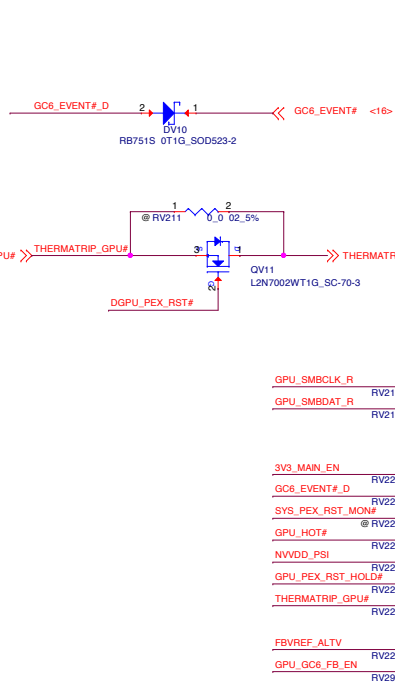
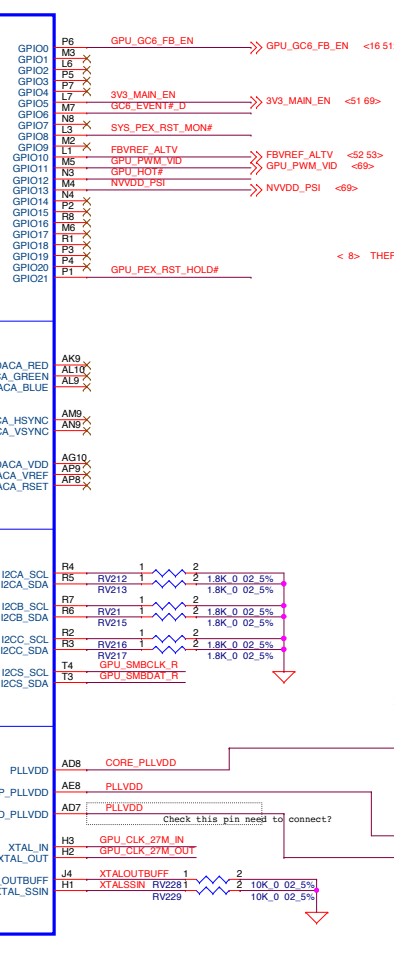
GPIO

DACS

PCI EXPRESS

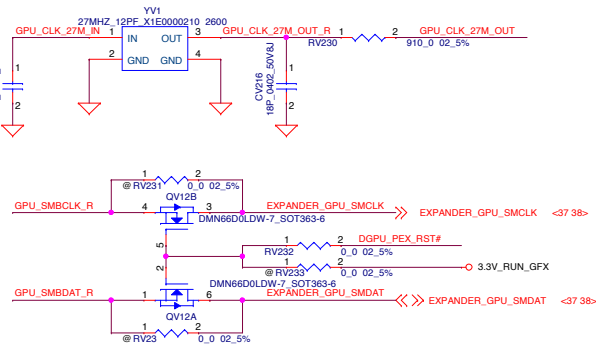
I2C

CLK



GC6 2.0 function

|               |                  |
|---------------|------------------|
| GPU_PWR_LEVEL |                  |
| LOW           | Low Performance  |
| HIGH          | High Performance |



| Capacitor Type                  | Population |
|---------------------------------|------------|
| 0.1uF 0402                      | 1 per ball |
| 4.7uF 0603                      | 1          |
| 22uF 0805                       | 1          |
| Bead 180 ohm (ESR=0.2 ohm) 0603 | 1          |

| Capacitor Type                  | Population |
|---------------------------------|------------|
| 0.1uF 0402                      | 1          |
| 22uF 0805                       | 1          |
| Bead 30 ohm (ESR=0.05 ohm) 0402 | 1          |

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Compal Electronics, Inc.

N17M PCIE,I2C,DAC,GPIO

LA-E153P

Document Number

Tuesday, June 28, 2016

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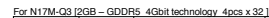
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| SMBUS_ALT_ADDR | Description           |
|----------------|-----------------------|
| 0              | 0x9E(Default)         |
| 1              | 0x9C(Multi-GPU usage) |

| VGA_DEVICE | Description   |
|------------|---|
| 0          | Non-Primary 3D Acceleration Device(Class Code 302h) |
| 1          | Primary Display or VGA Device(Class Code 300h)      |

| Resistor Value | Pull-up to VDD33 | Pull-down to GND |
|----------------|------------------|------------------|
| 4.99K          | 1000             | 0000             |
| 10K            | 1001             | 0001             |
| 15K            | 1010             | 0010             |
| 20K            | 1011             | 0011             |
| 24.9K          | 1100             | 0100             |
| 30.1K          | 1101             | 0101             |
| 34.8K          | 1110             | 0110             |
| 45.3K          | 1111             | 0111             |

| Speed Grade | Alert |
|-------------|-------|
| 5 Gbps      | N/A   |
| 5 Gbps      | N/A   |

\*

DEVID\_SEL/PCIE\_CFG default set 0 need refer Platform Update Notification for the latest configuration



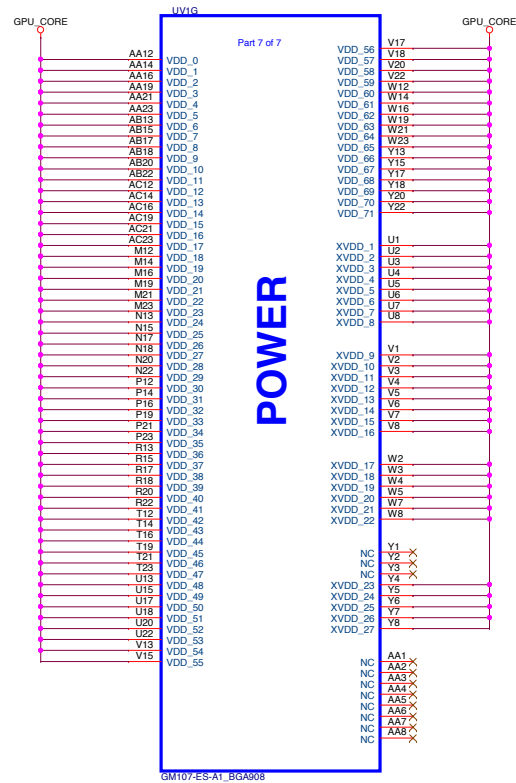
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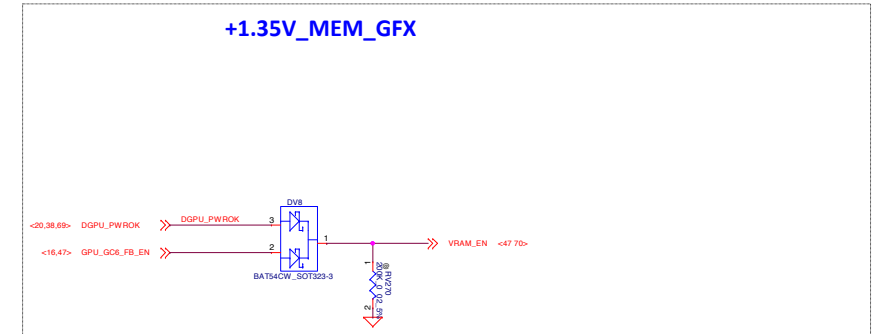
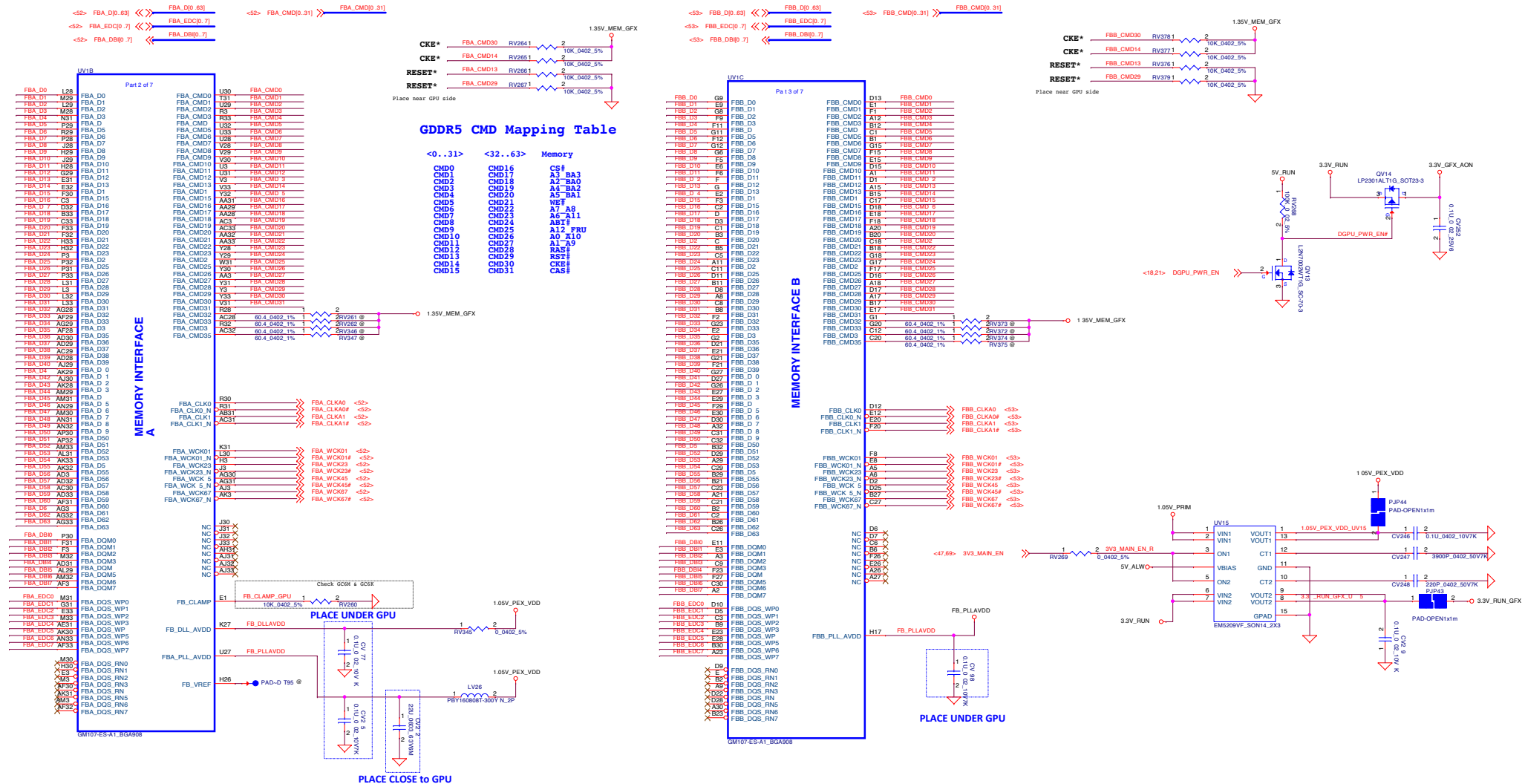


Caps on Power Side  
1UX8 4.7UX15 under GPU  
4.7UX5 22UX7 330UX1 near GPU



|                         |  |  |  |                          |  |  |  |                               |  |  |  |
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| Size                    |  |  |  | B                        |  |  |  | Rev                           |  |  |  |
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|                         |  |  |  | 50                       |  |  |  | of                            |  |  |  |
|                         |  |  |  | 7                        |  |  |  |                               |  |  |  |

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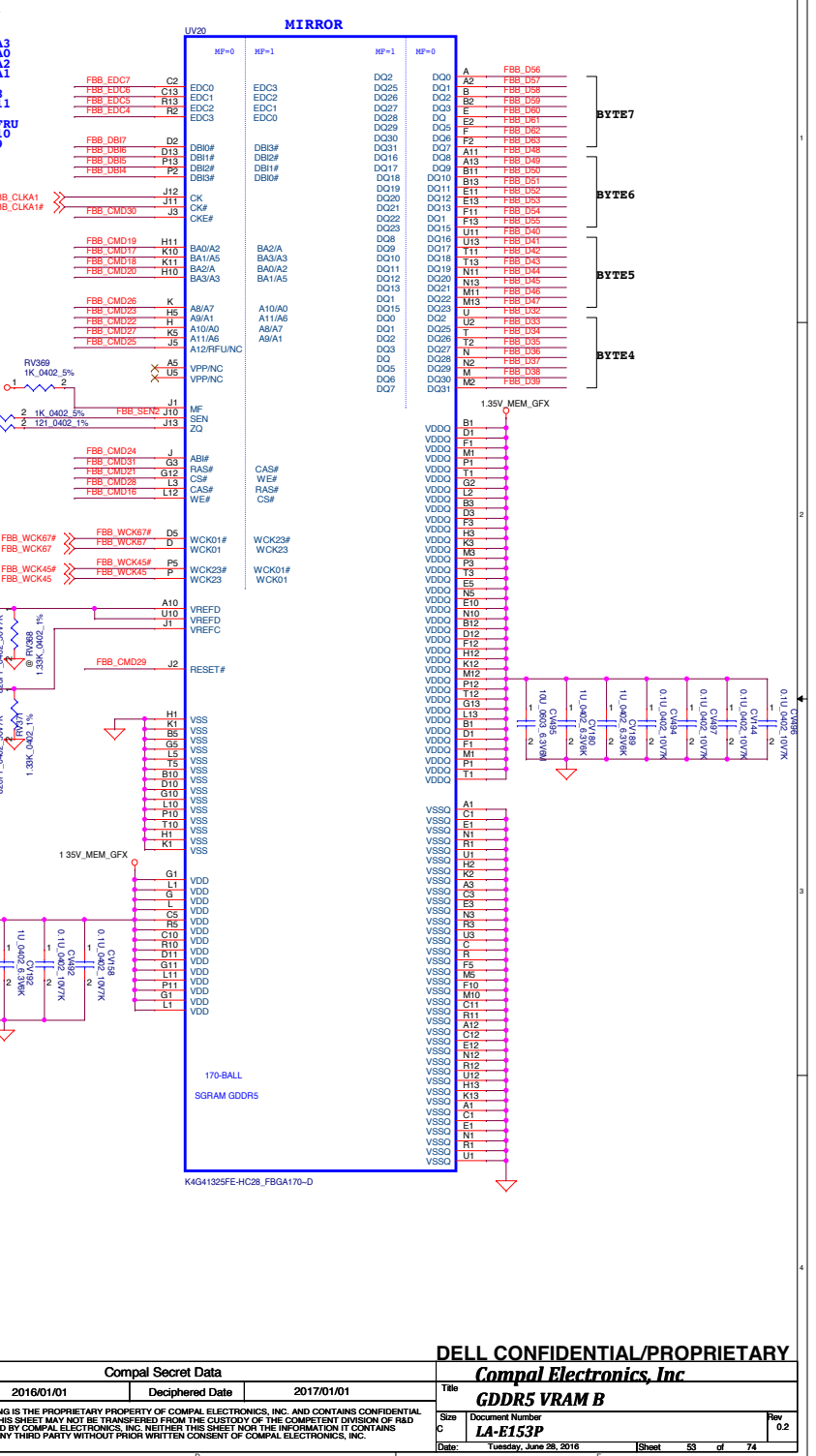
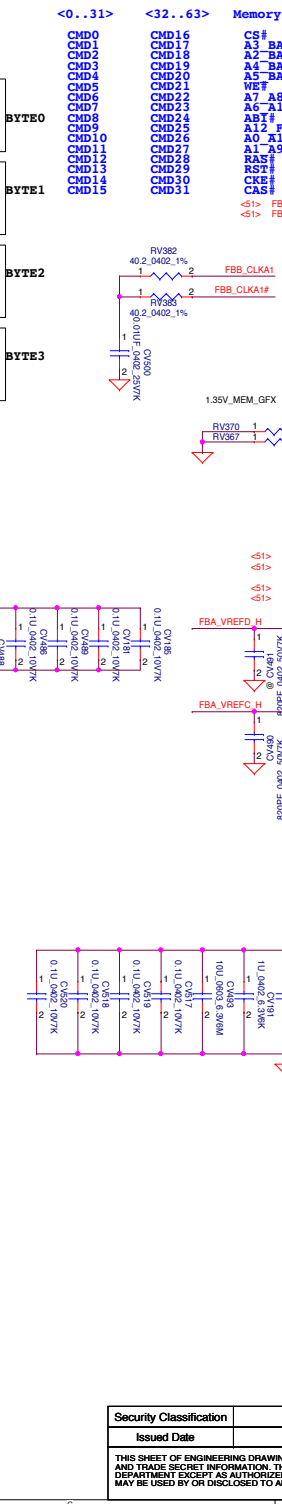
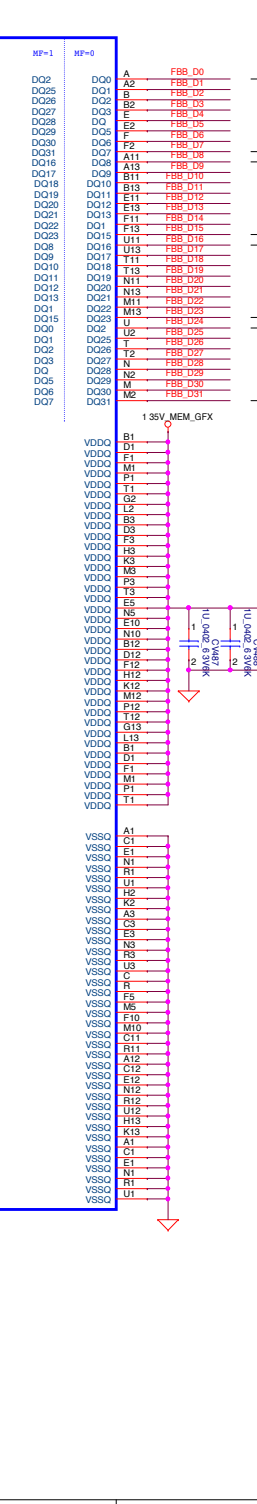
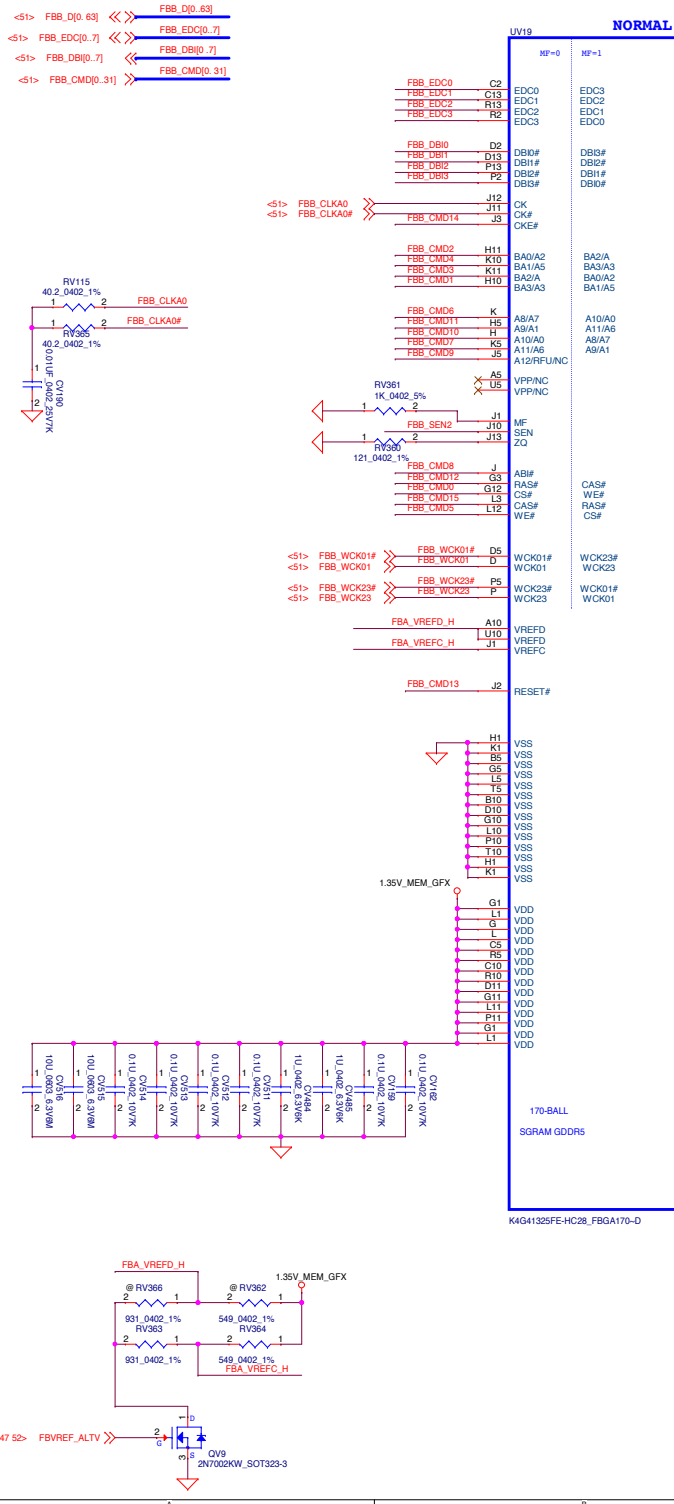








# GDDR5 CMD Mapping Table



**WWW.AliSaler.Com**



For power common schemati

|   |            |                        |            |  |                             |
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For power common schemati

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|   |            |                    |            | Sheet                    | 56 of 74                 |
|   |            |                    |            | Rev                      | 0.2                      |

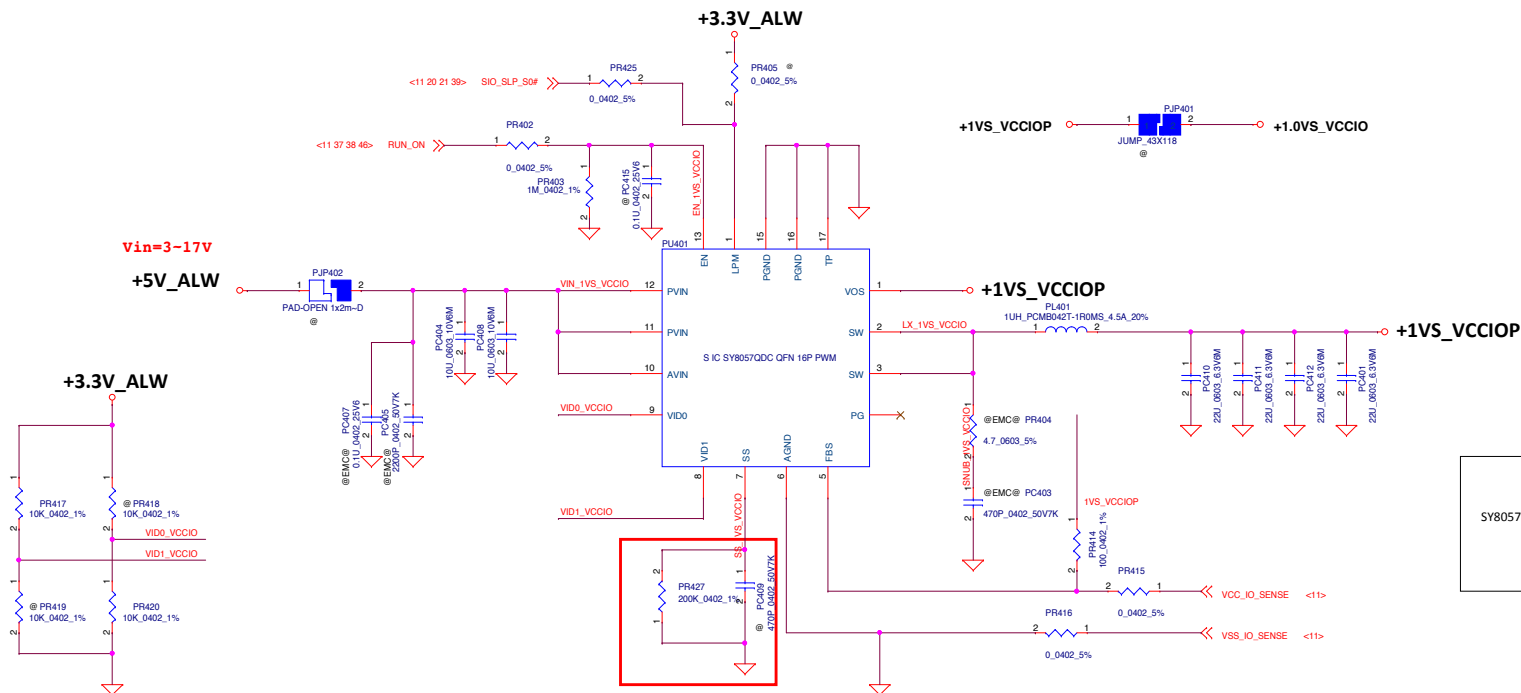










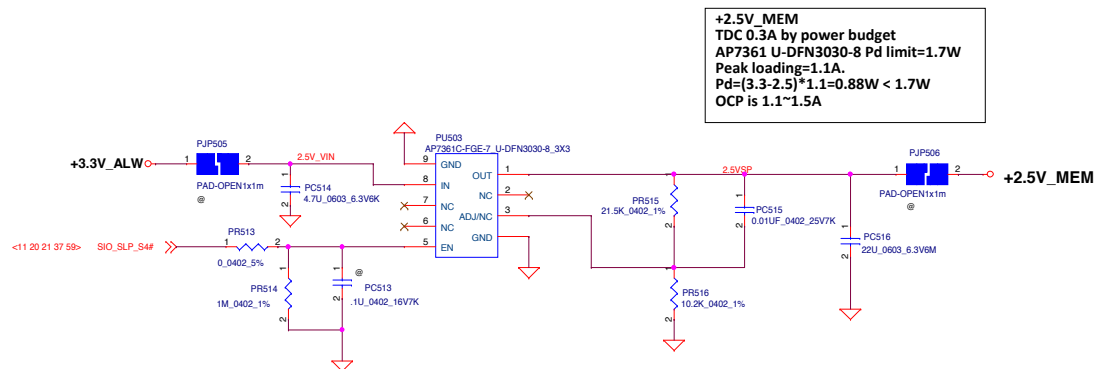
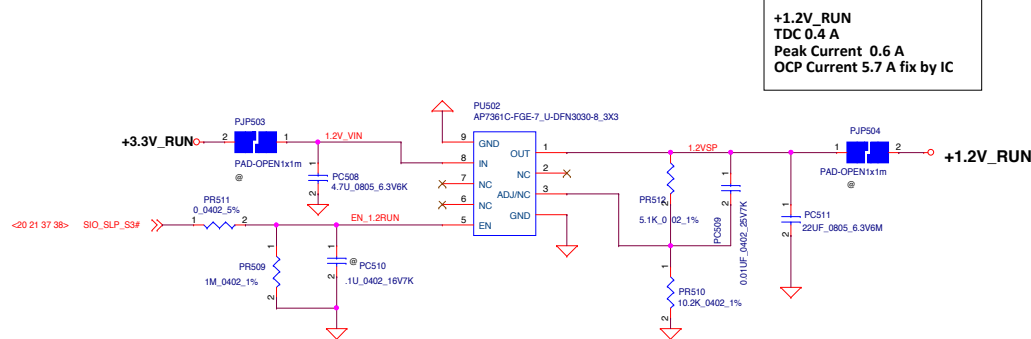
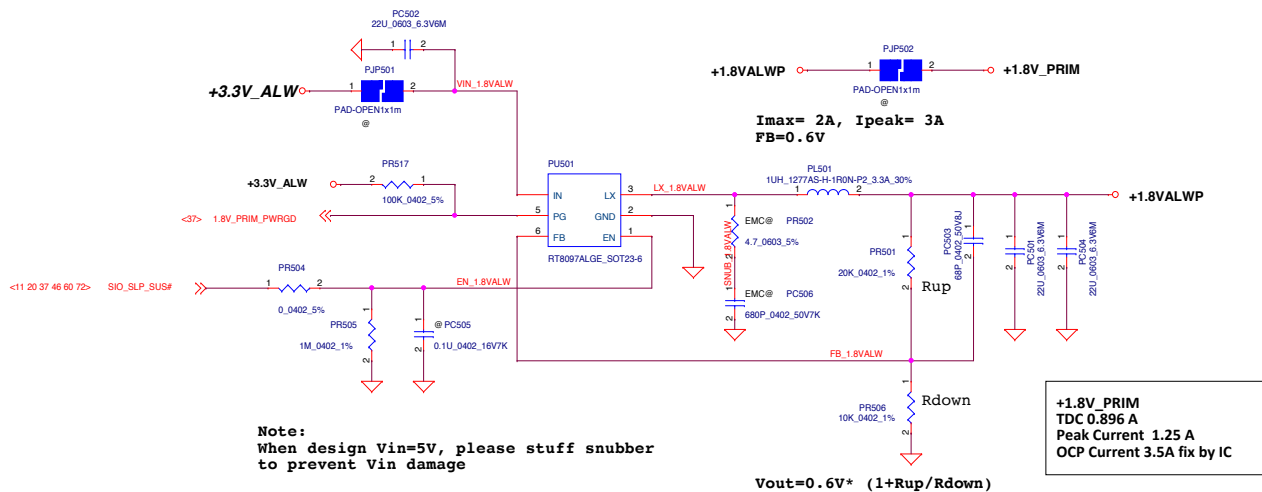


**+1.0VS\_VCCIO**  
TDC 3.9A  
Peak Current 5.5 A  
OCP Current 6.6 A Fix by IC  
TYP MAX

|        | LPM LOGIC | VID1 LOGIC | VID0 LOGIC | OUTPUT VOLTAGE |
|--------|-----------|------------|------------|----------------|
| SY8057 | 0         | X          | X          | 0(LPM)         |
|        | 1         | 0          | 0          | 0.85           |
|        | 1         | 0          | 1          | 0.875          |
|        | 1         | 1          | 0          | 0.95           |
|        | 1         | 1          | 1          | 0.975          |

Preset the different pull down resistor to choose the required power rail

(VCCIO/PCH/EDRAM/EOPIO applications.)  
RMODE>500k Vcc\_PRIM\_CORE.  
RMODE 200k Vcc\_IO.  
RMODE 0 Vcc\_EDRAM.

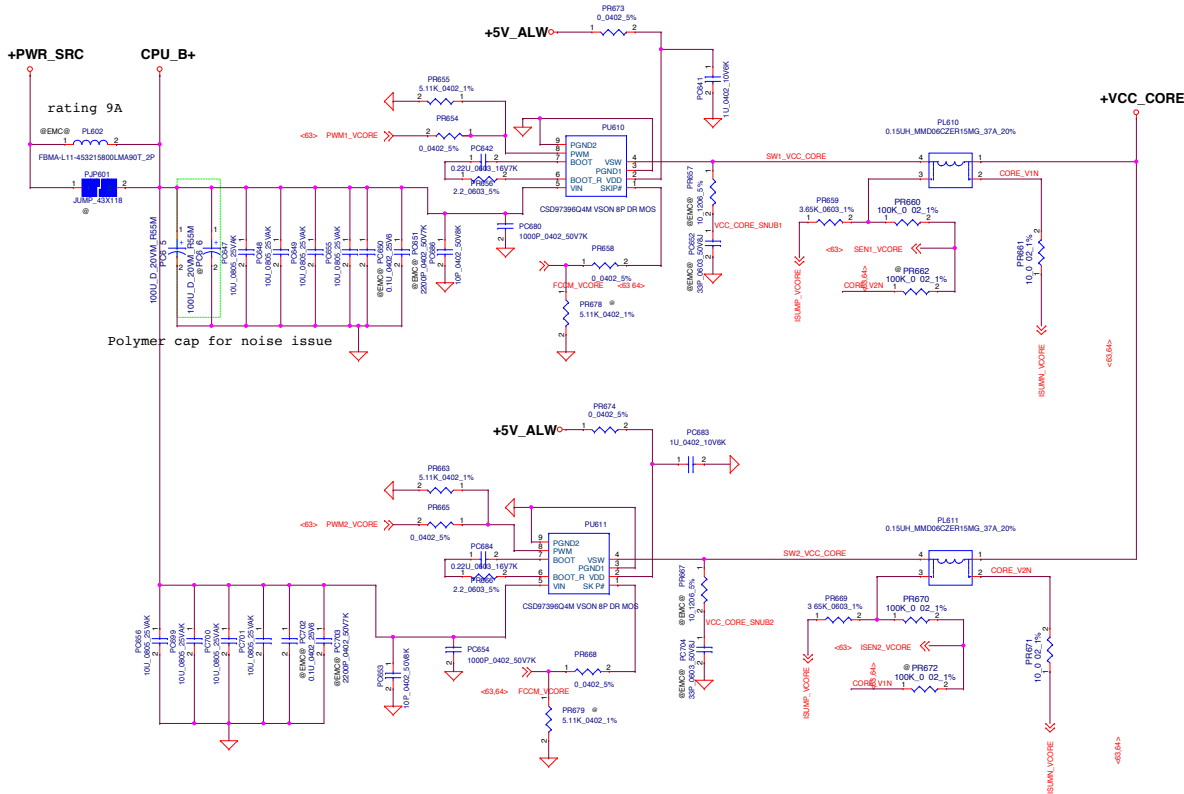


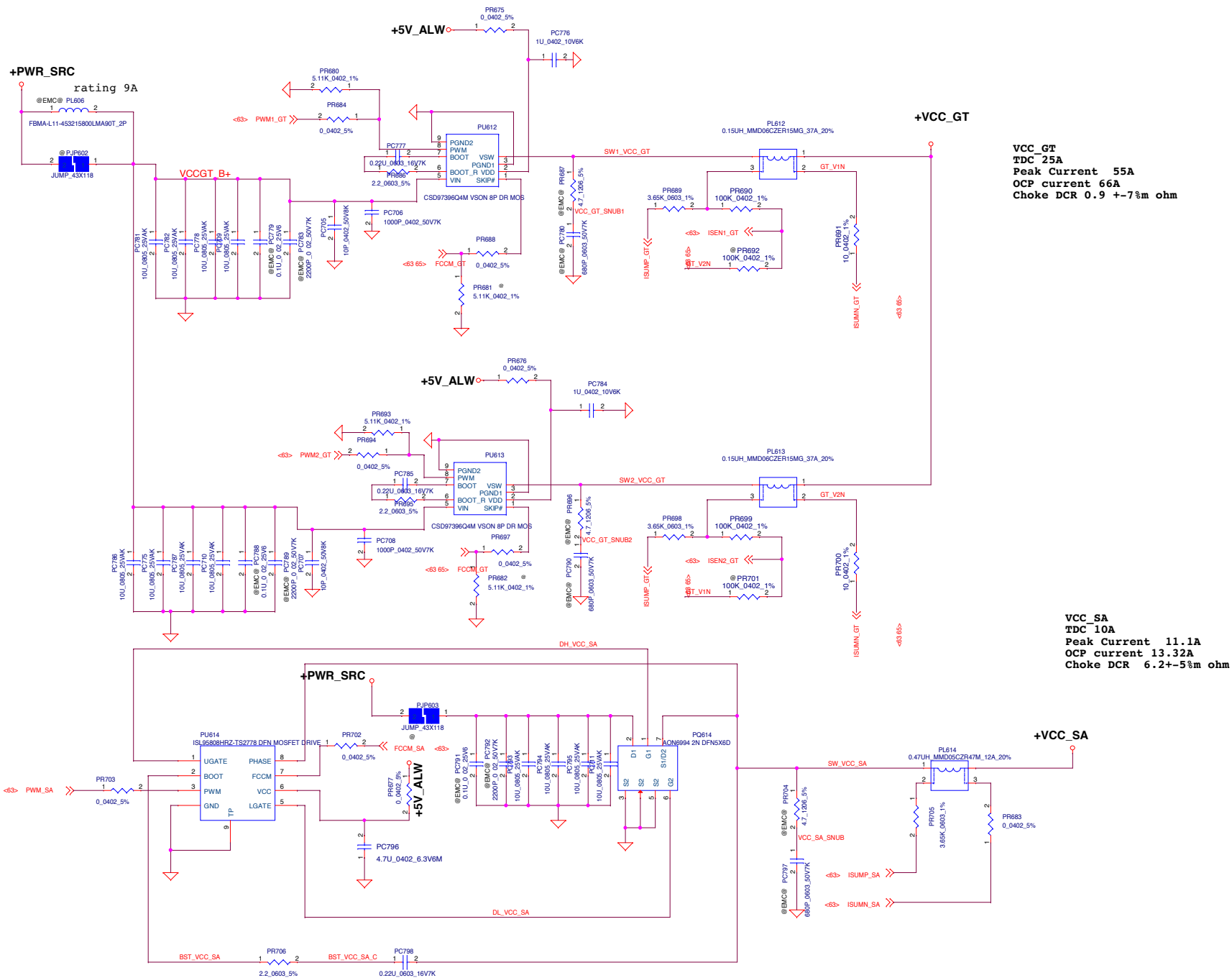
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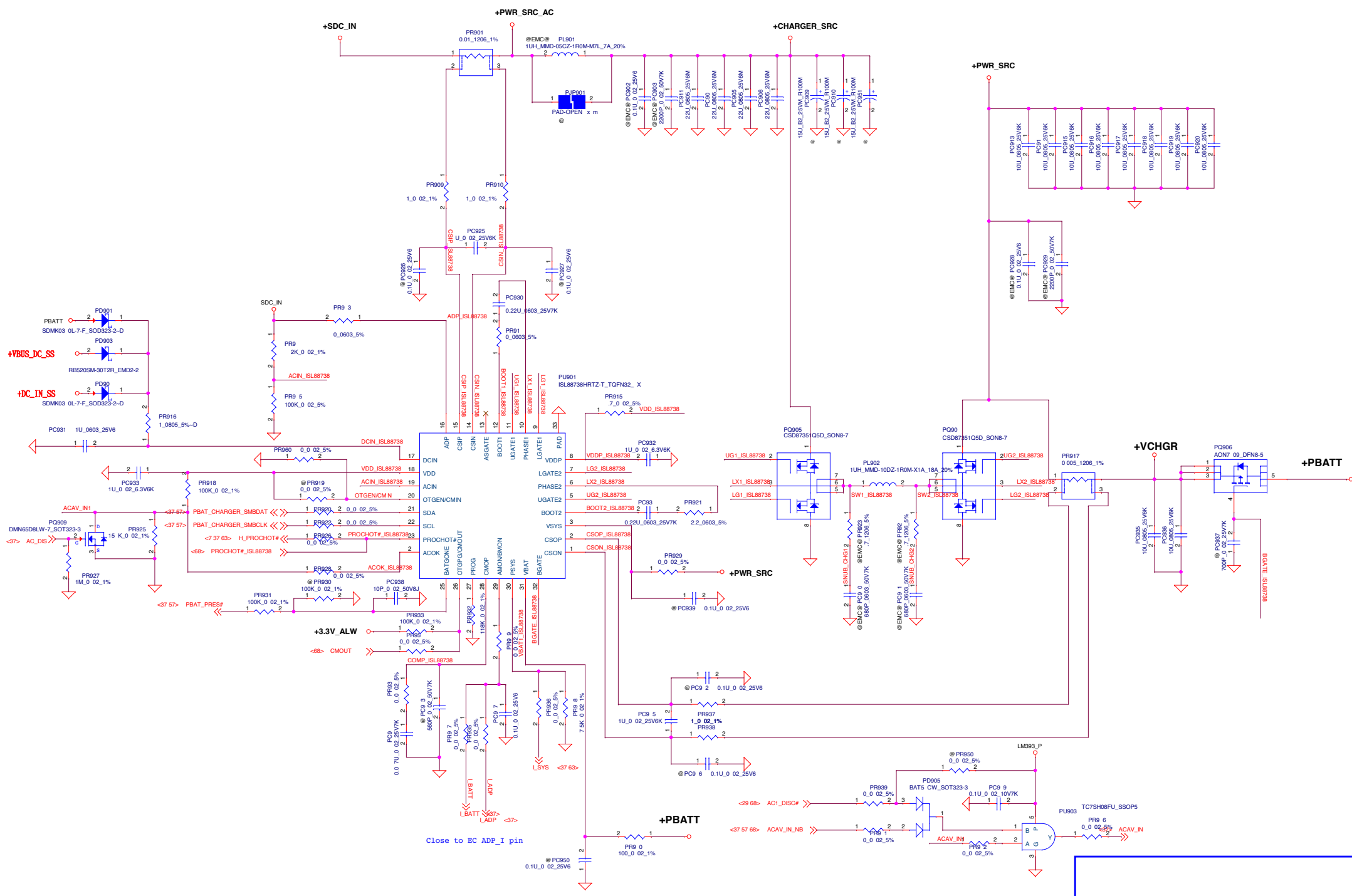
VCC\_core  
TDC 50A  
Peak Current 68A  
OCP current 81.6A  
Choke DCR 0.9 +-7% ohm





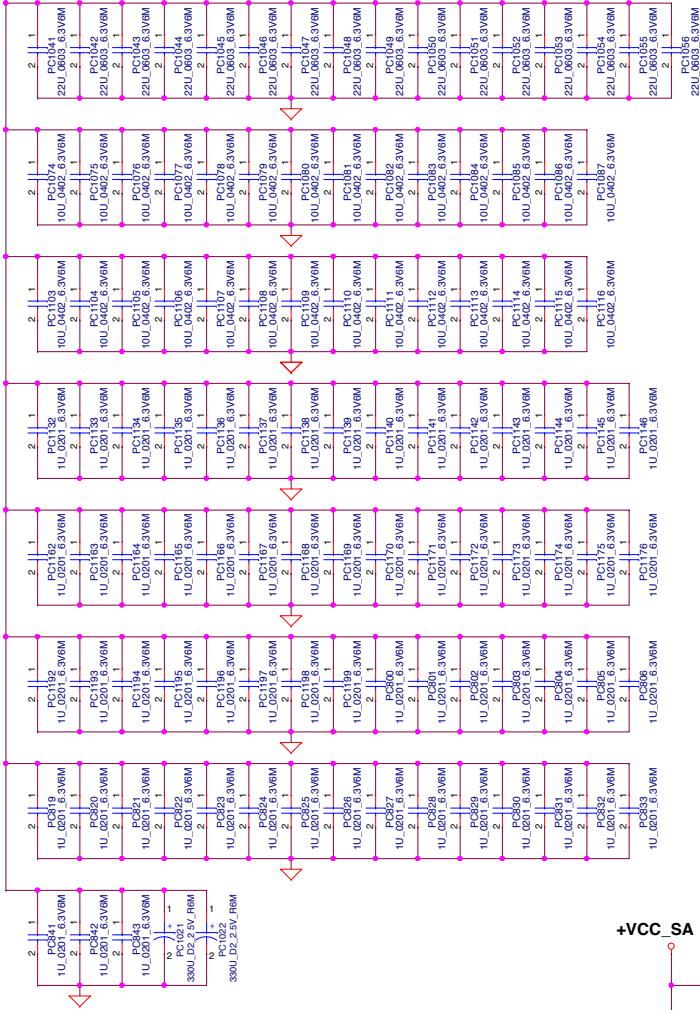
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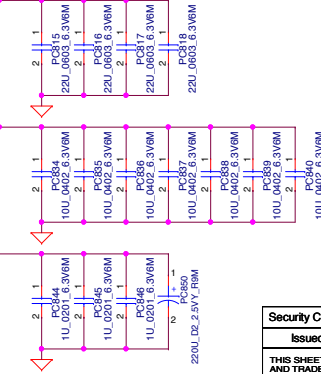
+VCC\_CORE

VCC\_CORE Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs + 10U\_0402\*28 pcs + 1U\_0201\*35 pcs  
Primary Side.  
22U\_0603 \* 8 pcs+330u\_D2\*2 pcs



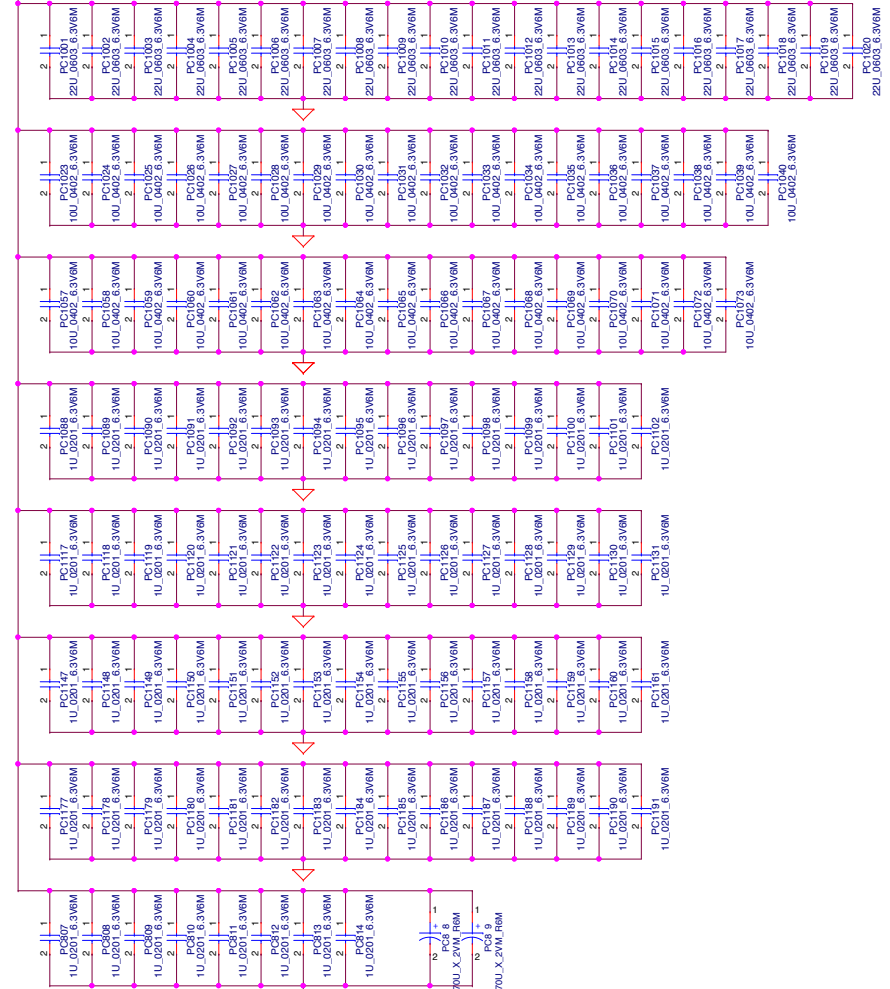
VCC\_SA Place on CPU  
Back Side.  
22U\_0603 \* 2 pcs + 10U\_0402\*7 pcs + 1U\_0201\*3 pcs  
Primary Side.  
22U\_0603 \* 2 pcs + 220u\_D2\*1 pcs

+VCC\_SA



+VCC\_GT

VCC\_GT Place on CPU  
Back Side.  
22U\_0603 \* 8 pcs +10U\_0402\*35 pcs +1U\_0201\*68 pcs  
Primary Side.  
22U\_0603 \* 12 pcs +470u\_D2\*2 pcs

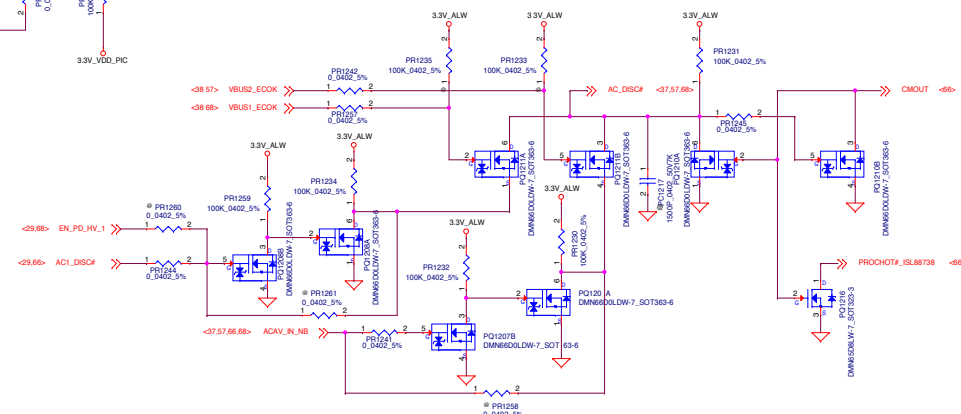
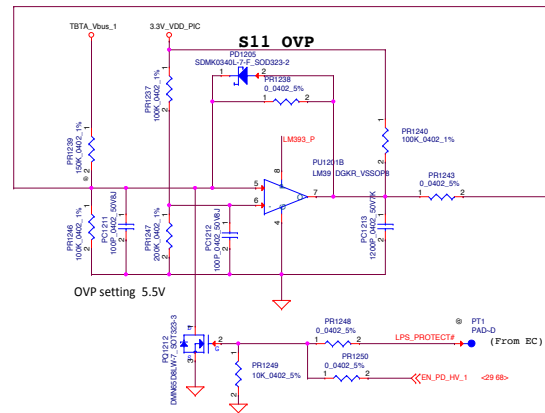
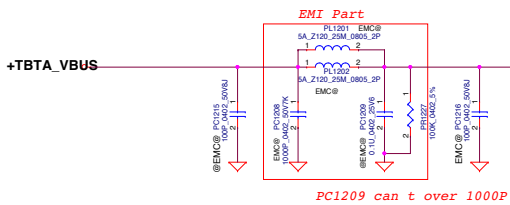
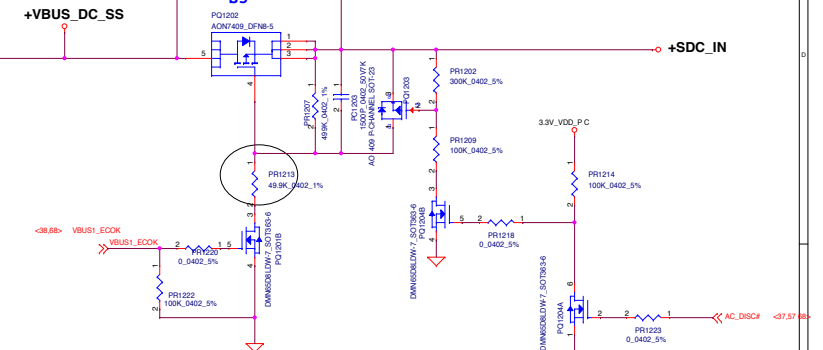
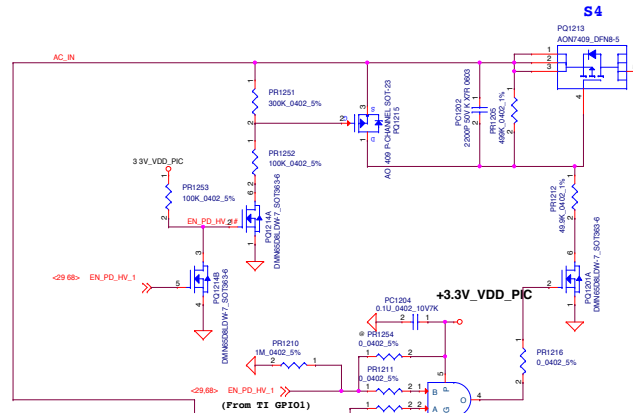
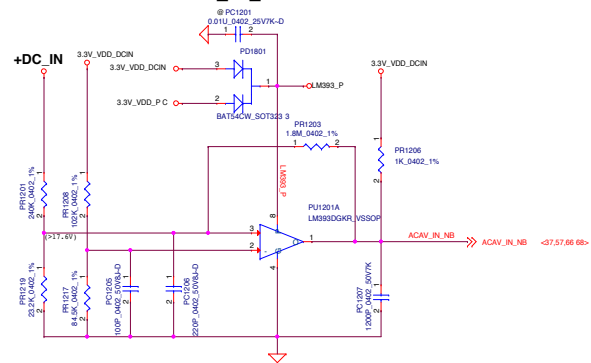


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$V_{boot} = V_{ref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$   
 $R_t = R_{refad} // (R_{boot} + R_{ref2})$   
 $V_{min} = V_{ref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$   
 $V_{max} = V_{ref} * R_{ref2} / [(R_{ref1} / R_{refad}) + R_{boot} + R_{ref2}]$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

#### PWM-VID Spec and component Values

| PWM-VID Spec | Config A | Config B | Config C |
|--------------|----------|----------|----------|
| Vmin         | 0.6V     | 0.6V     | 0.65V    |
| Vmax         | 1.2V     | 1.2V     | 1.15V    |
| Vboot        | 0.875V   | 0.9V     | 0.9V     |
| Voltage step | 6.25mV   | 6.25mV   | 25mV     |
| N of         | 96       | 96       | 24       |
| Vref1        | PR9      | 39K      | 20K      |
| Rboot        | PR5      | 39K      | 20K      |
| Rref2        | PR8      | 1.5K     | 2K       |
| Rref1        | PR10     | 30K      | 18K      |
| Rref2        | PR12     | 1.5K     | 0        |
| C            | PC8      | 1.5nf    | 2.7nf    |

**Module model information:**  
**RT8813A\_V1A for IC module**  
**RT8813A\_V1B for SW module**

Current Limit threshold setting  
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10 \mu\text{A}$   
 $I_{ripple} = (19-0.9) * 0.9 / (304.89 \text{ Khz} * 0.36 \mu\text{s}) = 7.811 \text{ A}$   
 $OCP = 54 \text{ A} / 2 = 27 \text{ A}$  per phase  
 $I_{valley} = 27 \text{ A} - 7.811 \text{ A} = 23.1 \text{ A}$

H-side MOS:TPCA8065  
 $R_{ds(on)} = 11.7 \text{ m}\Omega @ V_{gs} = 10 \text{ V}$   
 $9.4 \text{ m}\Omega @ V_{gs} = 4.5 \text{ V}$   
 $I_d: 16 \text{ A} @ T_a = 25 \text{ degC}$   
 L-side MOS:TPCA8057  
 $R_{ds(on)} = 2.0 \text{ m}\Omega @ V_{gs} = 10 \text{ V}$   
 $2.6-3.2 \text{ m}\Omega @ V_{gs} = 4.5 \text{ V}$   
 $I_d: 42 \text{ A} @ T_a = 25 \text{ degC}$

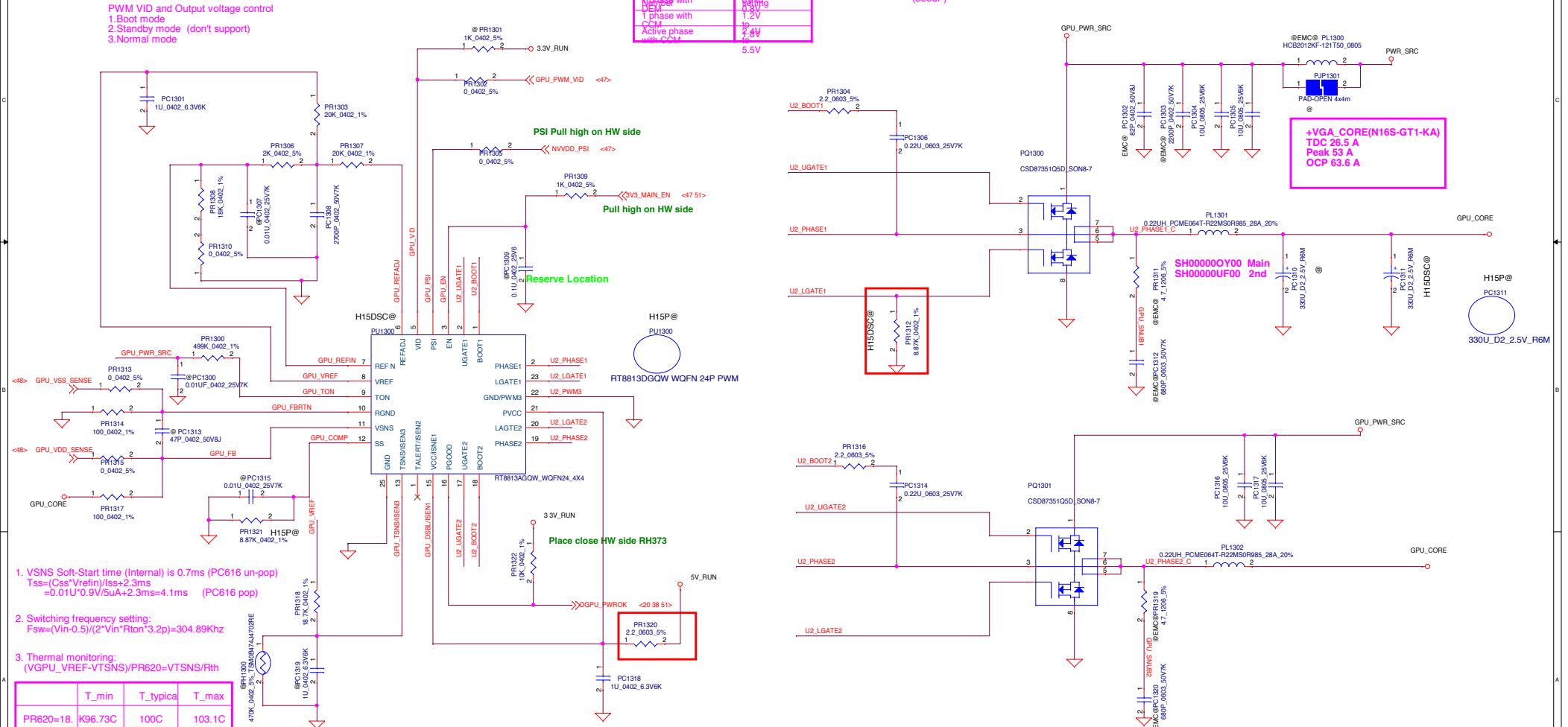
Choke: 0.36uH (Size:10\*10\*4)  
 $R_{dc} = 1.1 \text{ m}\Omega @ 5\%$   
 Heat Rating Current=30A  
 Saturation Current=50A

$C = 3 * 330 \mu\text{F} (9 \text{ m}\Omega) = 990 \mu\text{F}$   
 $V_{ripple} = I_{ripple} * ESR(\text{min}) = 7.811 \text{ A} * 3 \text{ m}\Omega = 23.4 \text{ mV}$

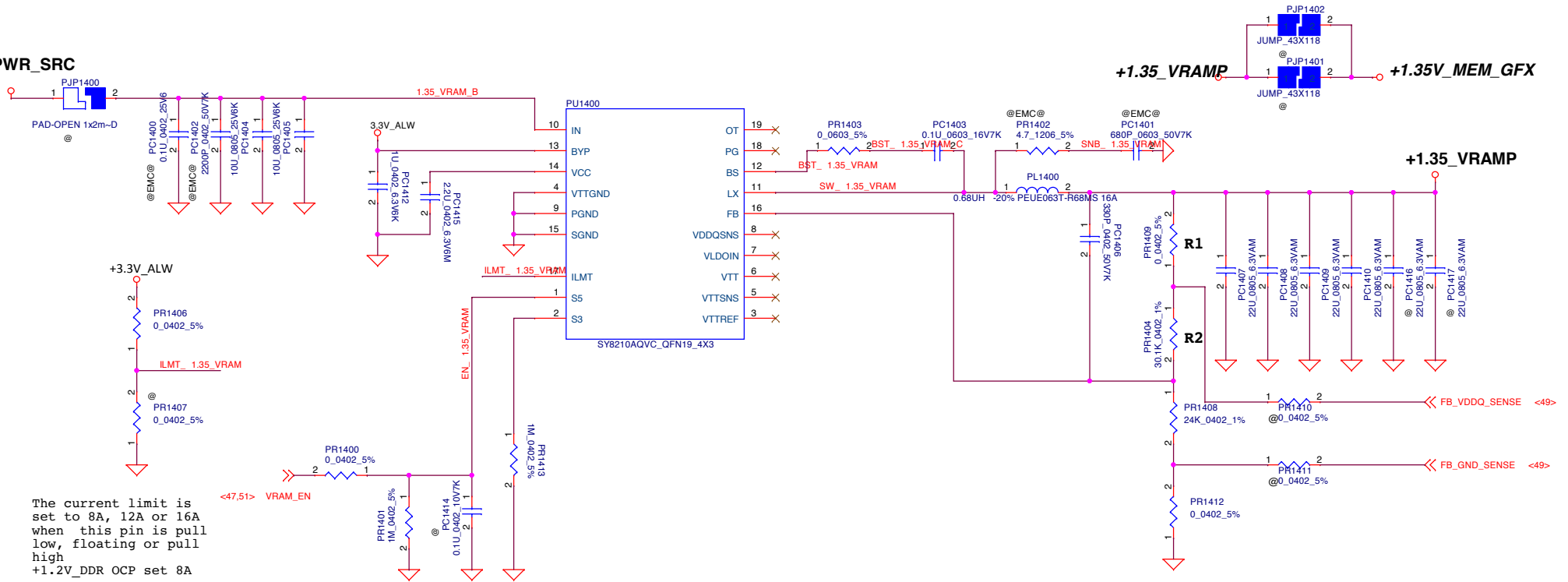
| Operation phase        | PSI Voltage setting |
|------------------------|---------------------|
| Normal phase with PWM  | 1.2V                |
| Standby phase with PWM | 1.2V                |
| Active phase with CCM  | 1.2V                |
|                        | 5.5V                |

Different VGA Chip (different EDP-Peak Current) need select different solution

| VGA Chip                             | N14P-GV     | N14P-GV2    | N14M-GS     | N14M-LP     | N14P-LP     | N14P-GE     | N14P-GS              | N14P-GT                |
|--------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------|------------------------|
| OpenVReg Configurations              | Config B    | Config B    | Config B    | Config B    | Config B    | Config B    | Config B             | Config B               |
| Rated TDP                            | 18W         | 25W         | 18W         | 13W         | 18.9W       | 25W         | 25.6W                | 35.5W                  |
| Power at Boost GPU Total at Tj=102C  | 25W         | 32W         | 25W         | 20W         | 23W         | N/A         | 30W                  | 40W                    |
| EDP-Continuous at Tj=102C            | 24A         | 32A         | 26A         | 22A         | 25A         | 27A         | 38A                  | 45A                    |
| EDP-Peak at Tj=102C                  | 35A         | 55A         | 45A         | 35A         | 35A         | 40A         | 60A                  | 75A                    |
| Istep max (Evaluation)               | 15A         | 27A         | 25A         | 20A         | 14A         | 12A         | 31.5A                | 35A                    |
| OCP Setting                          | 42A         | 66A         | 54A         | 42A         | 42A         | 48A         | 72A                  | 90A                    |
| Rusest                               | 8.96K       | 12.45K      | 10.7K       | 8.96K       | 8.96K       | 9.83K       | 8.3K                 | 9.39K                  |
| Recommendation                       | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H2L          | 2phase 1H2L            |
| Polymer Cap (330uF) Or OSCON (390uF) | 6mohm * 2   | 9mohm * 3   | 9mohm * 3   | 6mohm * 2   | 6mohm * 2   | 6mohm * 2   | 6mohm * 3 (L=0.22uH) | 4.5mohm * 3 (L=0.15uH) |



# +PWR\_SRC



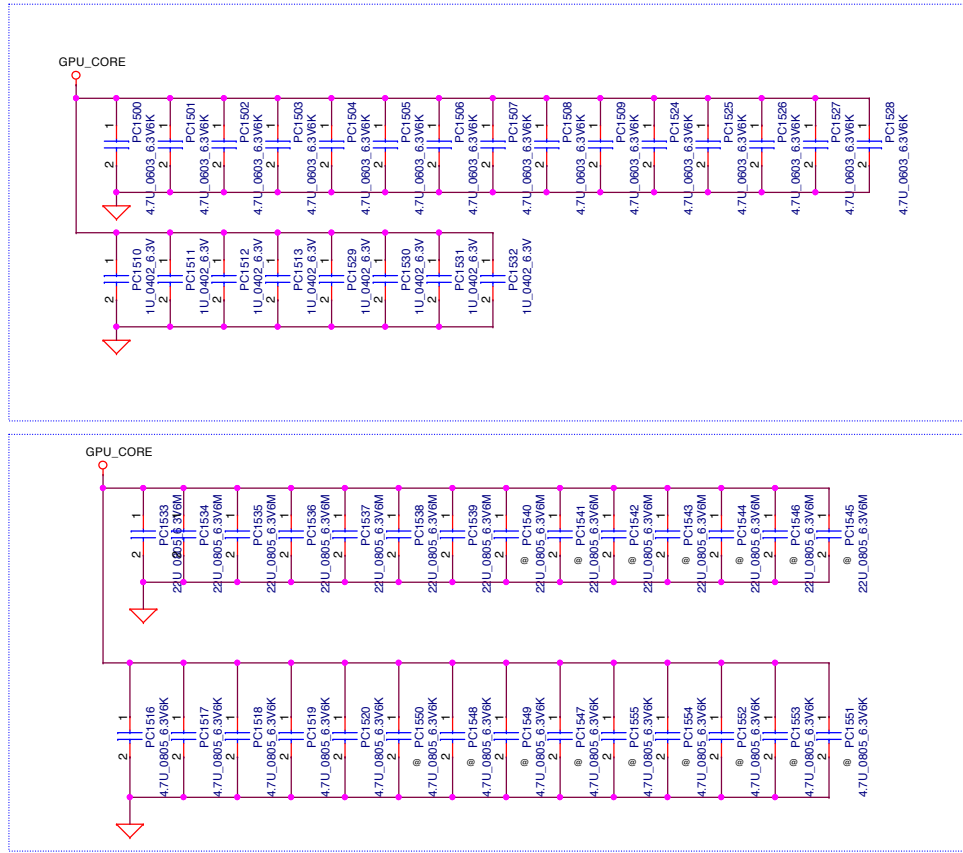
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GPU\_VRAM(SYX198D)

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nVidia GB4B-128 package  
Under GPU  
4.7uF 0603 \* 15  
1uF 0402 \* 8

nVidia GB4B-128 package  
Near GPU  
22uF 0805 \* 7  
4.7uF 0805 \* 5

|   |  |                    |  |                               |                 |
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# Version Change List ( P. I. R. List )

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|------|-------|-------|-----------|---------------|--|---|----------|
| 1    | 11    | HW    | 2016/5/27 | COMPAL        | S0ix(modern standy) support for VCCPLL_OC  | Pop RZ120 and Depop UZ34<br>Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1   | 0.2(X01) |
| 2    | 37    | HW    | 2016/5/27 | COMPAL        | Reserve PORT80_DET# PD resistance  | Reserve RE513 100k (SD028100380) to GND   | 0.2(X01) |
| 3    | 35    | HW    | 2016/6/1  | COMPAL        | Intel schematics reivew modify item  | CZ28,CZ29 change from 0.047uF to 0.01uF<br>CZ27 change from 0.1uF(0)_0201 to 10uF_0603  | 0.2(X01) |
| 4    | 45    | HW    | 2016/6/1  | COMPAL        | JLED1 pin define error   | JLED1 pin definition change   | 0.2(X01) |
| 5    | 39    | HW    | 2016/6/1  | COMPAL        | TPM change to NUVOTON  | Change TPM from Atmel to NUVOTON.   | 0.2(X01) |
| 6    | 35    | HW    | 2016/6/1  | COMPAL        | Intel reviwie result<br>(WWAN Coex feature support)                                | Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3<br>Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2<br>Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1 | 0.2(X01) |
| 7    | 35    | HW    | 2016/6/7  | COMPAL        | Debug card reserve   | Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX  | 0.2(X01) |
| 8    | 37    | HW    | 2016/6/7  | COMPAL        | For MEC5105K-D1-TN setting   | 1. Change UE1 to SA00009GL00<br>2. POP RE360,RE362<br>3. De-POP RE361   | 0.2(X01) |
| 9    | 35,32 | HW    | 2016/6/16 | COMPAL        | For EMC request  | De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268<br>modify from 22p to 47p and POP,Change LV1 to SM01000NY00                             | 0.2(X01) |
| 10   | 41    | HW    | 2016/6/16 | COMPAL        | BITS284924-HDD is still working after press<br>power button into S5 during POST.   | POP RN5   | 0.2(X01) |
| 11   | 39    | ME    | 2016/6/17 | COMPAL        | Connector change   | 1. JKBTP1 change to CVILU_CF5020FDORK-05-NH<br>2. JUSH1 change to CVILU_CF5026FDORK-05-NH<br>3. JIR1 change to ACES_50208-0060N-P01                         | 0.2(X01) |
| 12   | 36    | HW    | 2016/6/20 | COMPAL        | Vender suggest   | RA7,RA8 change to 16.2ohm   | 0.2(X01) |
| 13   | 37    | HW    | 2016/6/22 | COMPAL        | The posibility of GPIO map update  | Add RE514,RE515 for RTCRST_ON   | 0.2(X01) |
| 14   | 41    | HW    | 2016/6/22 | COMPAL        | BITS283552 - [BR_CSLP] FFS AP no function<br>when execute FF generator or shake SU | FFS VDD_IO change to +3.3V_RUN  | 0.2(X01) |
| 15   | 28    | HW    | 2016/6/22 | COMPAL        | TypeC USB Rx EQ change 1dB can PASS<br>USB RSG test                                | depop RT144, pop RT304  | 0.2(X01) |

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